Design IP DATA**SHEET**

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Host Controller IP for SD/eMMC Interface

Overview

Next-generation portable devices, such as smartphones and tablets, require more content capacity and bandwidth for video, photos, and music, as well as faster switching between applications and more responsive user interfaces. The eMMC 5.1 specification from JEDEC improves on the HS400 mode (operating at 400MB/s) by adding a command queuing engine (CQE).

The Cadence® Host Controller IP for SD 6.0 / eMMC 5.1 improves portable devices' OS performance, utilizing an efficient CQE. The CQE helps optimize the performance of frequent, small data transfers by eliminating overhead, thus improving the number of I/Os per second (IOPS). The Controller IP provides the logic to integrate a Secure Digital (SD) card into any system on chip (SoC) and assures straightforward connectivity with the de-facto standard SD memory cards and eMMC devices by being compliant with SD Host Controller Standard Specification version 6.0, Part E1 of the SDIO Specification version 4.1 of the SD Physical Layer Specification 6.1, SD Specifications: JEDEC eMMC 5.1 standard (JESD84-B51).

Support for all speeds up to UHS-I SDR104 and DDR50 guarantees compatibility with any card available on the market. For eMMC devices, the Controller IP supports all speeds defined in the eMMC 5.1 specification, including HS200 and HS400.

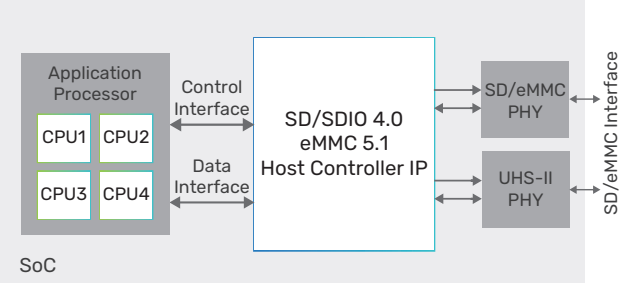

Figure 1: Example system-level block diagram

Benefits

- High bandwidth and low latency for best system performance
- Highly-integrated IP offering fast system integration and reduced design risk and cost
- Wide support of standards enables system flexibility for embedded and expandable storage

Key Features

- Command queuing engine (CQE) for reducing latency on small data transfers
- Supports Default Speed, High Speed, and UHS- I (SDR12, SDR25, SDR50, SDR104, and DDR50)
- Supports HS400 enhanced strobe for faster synchronization between the host and the device
- Selectable SDMA or ADMA2 (scatter-gather) engine
- Dual-Buffer mode optimized for throughput
- Supports all eMMC 5.1 speeds: SDR, DDR, HS200, and HS400
- Programmable 1/4/8-bit DAT bus width (in non-UHS-II modes)
- Sample clock tuning control logic for UHS-I SDR104

Product Details

The Cadence SD/SDIO 6.0 and eMMC 5.1 Host Controller IP works with SD memory cards and eMMC devices in a variety of possible applications, including cameras, card readers, mobile phones, tablets, and embedded systems.

BIU

The bus interface unit (BIU) provides status and configuration access to the internal registers, including the Slot Register Set (SRS), the Common Register Set (CRS), and the proprietary Host Register Set (HRS). An optional DMA engine is available for data streaming. The DMA engine can be configured as either Single Operation DMA (SDMA) or Advanced DMA (scatter-gather, ADMA2) as defined by the SD 4.0 Host Controller Specification.

CQE

The command queuing engine (CQE) module processes commands requested through CQ registers. It uses the Control and DMA Engine module to read and execute CQ tasks.

SCU

The slot control unit (SCU) is responsible for communicating with SD card or eMMC devices through an appropriate PHY.

CIU

The legacy SD/eMMC card interface unit (CIU) contains card clock dividers, Command/Response generation logic (CMD), and 1/4/8-bit data path logic (DAT).

FIU

The FIFO interface unit (FIU) implements control logic to manage data transactions between the SD card or eMMC

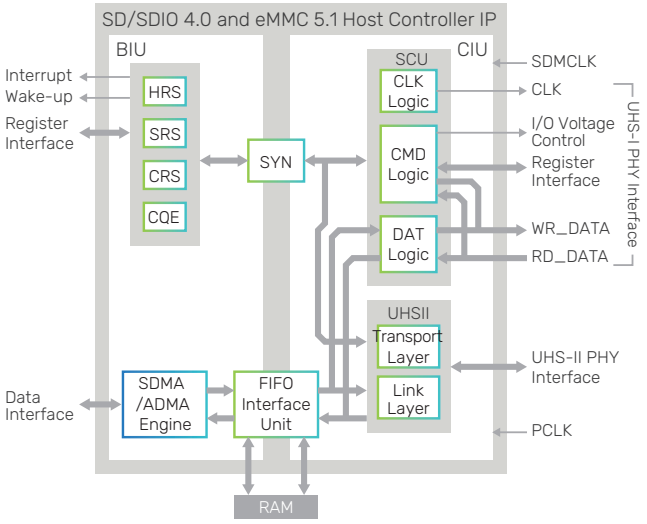

Figure 2: IP-level block diagram

device and system memory. For high-performance applications, dual-port RAM is configured as two virtual buffers, with one buffer dedicated to the BIU, while the other buffer is dedicated to the CIU. Both buffers can be accessed simultaneously. For low power, or reduced-silicon applications, single-port memory is configured as one virtual buffer that can be accessed consecutively by either the BIU or CIU. The FIU also features command queuing for improved performance on small data transfers.

Cadence SD Host Driver

A C source-code driver and testbench are available to reduce time to market and provide a vehicle to optimize your application. Compatibility with the SD specifications allows the Controller IP to work with third-party SD drivers such as the one embedded in Linux.

Availability

- Controller IP for SD 4.0 and eMMC 5.1
- Controller IP for SD 6.0 and eMMC 5.1

Related Products

- IP for SD 3.0 (UHS-I) and eMMC 5.1 (HS400) PHY

Deliverables

- Clean, readable, synthesizable Verilog RTL
- Synthesis scripts with SDC constraints file
- Documentation—design specification, integration guide, and release notes
- Verification testbench with test set

For more information, visit ip.cadence.com

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