Design IP Datasheet

# 32/25Gbps Multi-Link and Multi-Protocol PHY IP for TSMC 7nm FinFET

## Overview

The Cadence® 32/25Gbps Multi-Link and Multi-Protocol PHY IP for TSMC 7nm FinFET is a high-performance SerDes operating from 1.25Gbps to 32Gbps and specifically designed for infrastructure and data center applications. It features long-reach equalization capability at very low active and standby power. The SerDes offers very low latency for time-critical applications for enterprise-level data communications, networking, and storage systems.

The PHY IP provides extensive flexibility to mix and match protocols within the same macro. The PHY IP is designed to run PCI Express® (PCIe®), CXL, CCIX, 25G-KR, and 10G-KR. Multiple test features are embedded and easily accessible by the end user. A user-friendly graphical interface called EyeSurf™ provides convenient access to real-time and non-destructive eye scope and bathtubs for monitoring the bit error rate (BER) and the link performance during live traffic.

The PHY IP quickly and easily integrates into any system on chip (SoC) and connects seamlessly to Cadence controller for full flexibility. This minimizes time and risk of device development. It offers integrators the advanced capabilities, flexibilities, support for advanced, high-performance designs. This IP can be configured by Cadence to be a full, multi-protocol PHY or a PHY that supports a subset standards, where each protocol can be ordered as an

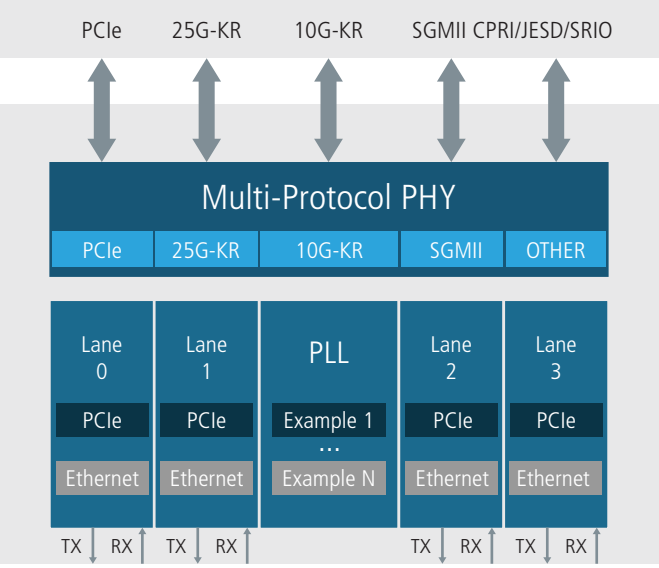


*Figure 1: Example System-Level Block Diagram*

## Benefits

- **Flexibility – Maximum flexibility and reconfigurability**
- **Maturity – Silicon proven and robust SerDes architecture**
- **Ease of use - Faster to integrate, bring up, and support**

## Key Features

- High-performance PHY for data center applications
- Low-latency, long-reach, and low-power modes
- Wide range of protocols that support networking, storage, and computing applications
- Multi-protocol support for application flexibility
- Non-destructive on-chip EyeSurf oscilloscope interface
- Extensive set of isolation, test modes, and loop-backs including APB and JTAG
- Supports 20-bit and 32-bit PIPE and non-PIPE interfaces
- Selectable serial pin polarity reversal for both transmit and receive paths

## Product Details

The PHY IP provides performance, reliability, and robustness for the most demanding applications.

The PHY IP is architected as a hard PHY macro with a Physical Media Attachment (PMA) layer and a soft Physical Coding Sublayer (PCS) available for various processes. The PHY IP supports a long-reach (LR) backplane with insertion loss in excess of 35+dB for rates up to 32G. It is specifically optimized to minimize end-to-end latency and power. Low-power modes are also supported (e.g., PCIe L1 substrates) for energy-efficient applications. For robustness, the PHY is designed to operate from -40°C to 125°C, it features superior ESD protection, and is designed to exceed the stringent reliability requirements of data center applications.

The PCS complies with the latest PCIe PIPE specification and provides support for the dynamic equalization features of different interface protocols. The PHY IP is designed for handling multi-protocols on one single PHY macro (see table below).

## PHY Architecture

The PHY IP is designed with a multi-link lane-based architecture, providing greater control over floorplanning, placement, packaging, and I/O integration than other hard PHY solutions, while maintaining the reliability and ease of use associated with GDSII macros.

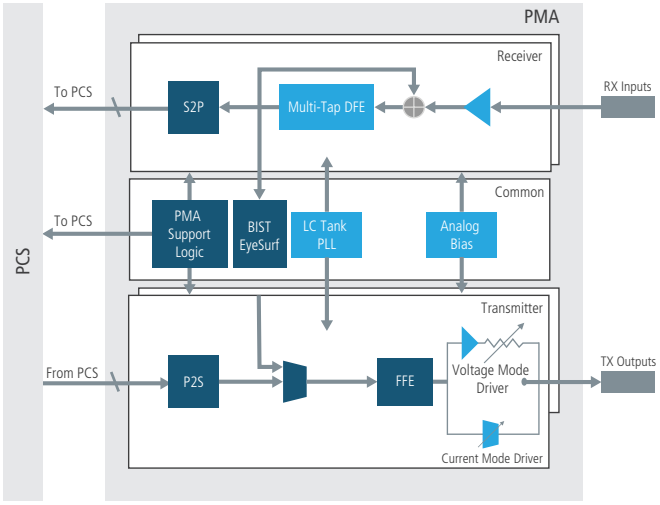


*Figure 2: IP-Level Block Diagram*

## Availability

The PHY IP is available with various configurations and supports the following protocols:

| Protocol* | Data Rate (Gbps/Lane) | Process Node |
|---|---|---|
| CXL | Up to 32 | 7nm FinFET |
| PCIe 5.0/4.0/3.0/2.0/1.0 | Up to 32 | 7nm FinFET |
| 25G-KR | Up to 26.5625 | 7nm FinFET |
| 10G-KR | 10.3125 | 7nm FinFET |
| QSGMII/SGMII | 5/1.25 | 7nm FinFET |

*Base product supports one protocol. Additional protocol support available as options.

## Related Products

- Cadence Controller IP for Cache Coherent Interconnect for Accelerators (CCIX)
- Cadence Controller IP for PCIe 5.0, 4.0, 3.0, 2.0, 1.0
- Cadence IP for Multi-Protocol PCS

## Deliverables

- Integration Views: Verilog behavioral model, GDSII, CDL, and power models
- Synthesizable RTL
- DFT-Verilog netlists with SS/FF, CTL, and BSDL
- Reference Verilog testbenches used for generating SoC-level VCD ATE test patterns for PHY
- IBIS-AMI kit
- Documentation: XML, integration and user guide, release notes
- Test boards available on demand

For more information, visit ip.cadence.com.

cadence®

Cadence software, hardware and semiconductor IP enable electronic systems and semiconductor companies to create the innovative end products that are transforming the way people live, work, and play. The company's Intelligent System Design strategy helps customers develop differentiated products—from chips to boards to intelligent systems. **www.cadence.com**