Design IP Brochure

PHY IP for DisplayPort/Embedded DisplayPort TX

Overview

Display requirements for system-on-chip (SoC) designs are becoming increasingly demanding, and must support increasing bandwidth that must be optimized for cost- and power-sensitive mobile, wireless IoT, and consumer designs.

The Cadence® PHY IP for DisplayPort/Embedded DisplayPort TX provides a configurable PHY IP that simplifies the design process without compromising performance, power, or silicon die area. The PHY IP is a lower-active and low-leakage power design crafted for mobile, wireless IoT, and consumer designs.

The PHY IP is a derivative design from a successful and proven Cadence 10Gbps multi-protocol multi-link PHY, carrying all the good attributes from original architecture (low power, flexible configurability, ease of use) with further optimization on reducing the IP area. The PHY IP provides a raw SerDes interface for controller interface.

The PHY IP is architected to quickly and easily integrate into any SoC, and to connect seamlessly to Cadence or third-party controllers. It provides a cost-effective, versatile, and low-power solution for demanding applications. It offers SoC integrators the advanced capabilities, flexibility, and support that meet the requirements of high-performance designs.

The PHY IP is part of the comprehensive Cadence Design IP portfolio comprised of interface, memory, analog, and system and peripheral IP.

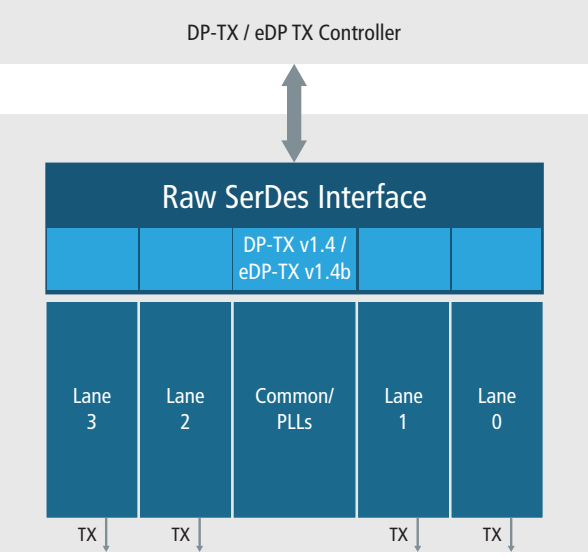

Figure 1: Example System-Level Block Diagram

Benefits

- **Optimum SoC configurability**
- **Optimized PPA for mobile and consumer applications**
- **Extensive BIST and DFT enable ease of integration, faster bring-up, and quick debugging**

Key Features

- DisplayPort and Embedded DisplayPort v1.4
- Support RBR, HBR, HBR2, HBR3 rates for DisplayPort and UI_Rate_1 through UI_Rate_8 for Embedded DisplayPort
- Support wide range of reference clock rates
- Support both internal and external clock sources
- Automatic calibration of on-chip termination resistors
- Flexible x1/x2/x4 configuration support single/dual links in one macro
- AUX/HPD function available in separate macro
- SCAN, BIST, and loopback functions

Product Details

The PHY IP is a hard PHY macro available for TSMC processes. I/O pads and ESD structures are included. It is designed to easily integrate with a Cadence Controller IP for DisplayPort or any third-party controller with a raw interface.

PHY Architecture

The PHY IP macro consists of a Physical Media Attachment (PMA) layer with a raw SerDes interface. The PHY IP is highly configurable, allowing the PHY to be easily configured to your specific needs.

The PHY IP is designed with a lane-based architecture featuring flexible x1, x2, and x4 configuration that could support single/dual DisplayPort/embedded DisplayPort links in one macro.

The architecture partitions the PMA core into different primary sub-modules: common blocks/PLLs and transmitter modules. The common PLL module also provides the interface between SCAN, AMBA bus, and JTAG and analog test including BIST, ABT, Scan, JTAG control, and PMA support logic functions.

The transmitter module converts parallel data from the raw SerDes interface to a serial data stream.

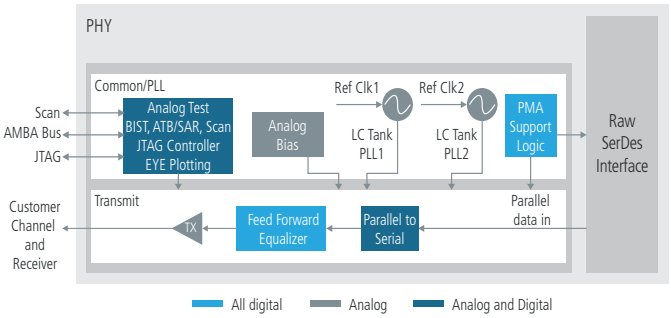

Figure 2: IP-Level Block Diagram

Availability

The PHY IP is available with support for the following process nodes:

Process node	Speed
12FFC	8.1 Gbps

Related Products

- Controller IP for DisplayPort v1.4

Deliverables

- Standard integration views: LEF abstract, timing views (.LIB), behavioral model (Verily), gate-level netlists (plural, SDF, DRC, LVS), ANT reports, and GDSII layout and layer map
- Synthesizable soft layer (primarily isolation logic) with SDC
- Complete documentation including user guide, integration guide, and programmer guide
- High Volume Manufacturing (HVM) kit
- Testboards available upon request

For more information, visit ip.cadence.com

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