Your cell phone works almost everywhere you can take it. On your phone, you can buy shoes from Bangladesh and download a movie from who knows where and watch a video about how to change your car battery. Your printer is connected to your laptop, which is connected to your home or work network. Even your refrigerator, thermostat, and light switch in the living room are all connected to your smart home assistant, which is connected to your phone, which is connected to the internet.

And yet, these connections can be imperfect. Note the word “almost” in the first sentence; the connectivity generation known as 4G (the fourth generation) almost—but not quite—does the job. Doing anything in “real time” on 4G can be unreliable; digital connectivity is often the culprit when your device fails. Entire market segments can’t take advantage of 4G technology. For example, the automotive market can’t rely on 4G to connect cars to the ambient infrastructure (V2I), to each other (V2V), or anything else (V2X), because instantaneous connectivity is a requirement.

This is why 5G has been in development for quite some time, and the reality of 5G is just around the corner. 5G brings three new features to connected communication: greater speed (to move more data), lower latency (to be more responsive), and the ability to connect a lot more devices at once (for sensors and smart devices). With the development of 5G comes the need for chip designers to work with this new technology, with low power and high performance in their processors as the priority. Cadence® Tensilica® ConnX B20 DSPs are a great step in that direction.

What Is 5G?

Like other networks, 5G networks use a system of cell sites that divide their territory into sectors and send data through radio waves. Each cell site must be connected to a network backbone. 5G networks must be smarter than previous systems, as well, since they’re handling many more, smaller cells.

To get super-high, multi-gigabit speeds, carriers will have to use much higher frequencies, known as millimeter waves (mmW). In the existing cellular bands, only relatively narrow channels are available because that spectrum is so busy and heavily used. But up at 28GHz and 39GHz, there are broad swaths of spectrum available to create big channels for very high speeds.

Those bands have been used before for connecting basestations to the internet, but they haven’t been used for consumer devices, because the handheld processing power and miniaturized antennas weren’t available. Another drawback to using mmW wave signals is that they drop off faster with distance than lower frequency signals do, and the massive amount of data they transfer will require more connections to landline internet. mmW signals also cannot penetrate buildings, walls, and mountain ranges very well. So, to solve these challenges, cellular providers will have to use many smaller, lower-power basestations (generally outputting 2W – 10W) rather than fewer, more powerful macrocells (which output 20W – 40W) to offer the multi-gigabit speeds that mmW networks promise.
With the launch of 5G in practice, IoT devices will see longer battery life, because of lower-power radio and more efficient processing of data in their digital systems. Multi-core processor solutions must reach throughput requirements with the fewer cores the better, so higher performance per core in these user devices is key.

Next-Generation 5G Technology

Typically, general-purpose CPUs are not ideal for special-function processing like 5G technology because they are inefficient at processing these algorithms and consequently consume too much power. That’s why specialized processors have been in development for years. Specialized DSPs like the Tensilica ConnX DSPs can process sensor data in highly parallel operations, matched to the data widths needed, that are much more efficient than a CPU and result in lower cost/size solutions. This is essential to keep power requirements within the limits allowed for 5G.

Some of the things you should look for when evaluating a new processor—particularly DSPs that you can add to your system-on-chip (SoC) design—include:

**Performance:** The DSP must finish its work in as few cycles as possible and at a faster clock speed.

**Memory:** The DSP must be designed to reach higher clock speeds with larger memories.

**Low Energy:** The DSP must finish the same work in fewer cycles and be power efficient so that many can be deployed if needed and not cause heating issues in the system.

**Low Cost:** The DSP must be as small as possible, resulting in lower cost.

The Tensilica ConnX B20 DSP meets all these needs for 5G technology, with the addition of an advanced optimizing compiler, optimized math libraries and application examples, and Eclipse IDE for full development, with debug and profiling on an ISS or JTAG target.

Even in the world of sensor processing, there’s no one-size-fits-all solution. Look for a family of compatible processors so you have the flexibility to pick just the features you need for your application. Cadence has already introduced several Tensilica ConnX DSPs—and you can expect that we will continue enhancing them to meet the computational requirements in the years ahead.