Design IP Datasheet

# Combo PHY IP for Storage

## Overview

The Cadence® Combo PHY IP for Storage is an all-digital soft PHY for NAND Flash, SD/eMMC, and xSPI Flash protocols. The DFI 3.0 interface has been specifically adopted for flash applications. An Arm® AMBA® AXI or APB register interface is used for configuration and calibration of the PHY settings.

Integration of the soft PHY enables the highest clock rates without the need for a faster reference clock, which in turn allows the following benefits: simplification of system-on-chip (SoC) designs, reduced number of clock domains, and power savings. The PHY supports speeds up to 600MHz and is structured so that future clock rate increases can be easily accommodated. The PHY contains a per-bit deskew mechanism, which improves the data window for the highest speed modes.

The Combo PHY IP for Storage supports all ONFI speed modes defined in the ONFI 4.1 specification and is backwards compatible to all previous ONFI specifications. The Combo PHY IP for Storage supports also Toggle 1 and Toggle 2 interfaces (including legacy asynchronous interface), SD (legacy/UHS-I), eMMC 5.1 JESD84-B51, and JESD 251 (xSPI), as well as legacy Multiple-SPI devices with Single/Dual/Quad interfaces.

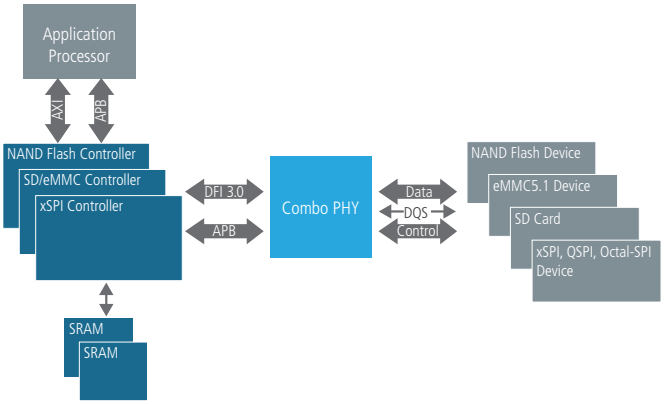


*Figure 1: Example System-Level Block Diagram*

## Benefits

- Flexibility—Can be used for many flash interfaces
- Simplicity—Using soft PHY simplifies SoC timing design
- High performance—Allows up to 600MHz
- Low-risk, proven design—Based on Cadence Denali® LPDDR3 PHY IP

The Combo PHY IP for Storage is architected to quickly and easily integrate into any SoC, and to connect seamlessly to the Cadence Controller IP for NAND Flash, Controller IP for SD/eMMC, and/or Controller IP for xSPI, or to a third-party controller using the DFI 3.0 interface.

The Combo PHY IP for Storage offers an automated design flow with advanced synthesis and static timing analysis (STA) scripts, which permits RTL-to-placed gates in an easy process.

## Key Features

- Supports ONFI 4.1, Toggle 1, 2, xSPI, and eMMC5.1 devices and SD3.0 cards
- Fully digital soft PHY implementation
- Integrated DLL supports speeds up to 600MHz
- DFI 3.0 interface adopted for flash
- Includes per-bit deskew mechanism
- Register interface for PHY programming
- Loopback, DFT
- DFI with 1:2 clock ratio support

## Product Details

The Combo PHY IP for Storage is a single module that encapsulates all functionality required to interface to external NAND Flash, xSPI, eMMC devices, and SD cards. It is compatible with all major NAND Flash devices, QSPI/Octal-SPI/xSPI devices, eMMC devices, and SD cards. There is a standard APB register interface for setup, configuration, and calibration of the flash interface. The Combo PHY IP for Storage is based on the proven Denali LPDDR3 PHY IP design, widely deployed across a range of silicon nodes.

## Digital DLL

The Combo PHY IP for Storage contains logic that, in conjunction with I/O cell circuitry, addresses the timing requirements for data transfers between the ASIC and asynchronous flash devices. The delay compensation circuit was designed with the following features:

- Programmable read clock delay specified as a percentage of a clock cycle
- Programmable write data delays specified as percentages of a clock cycle
- Delay compensation circuit, re-sync circuitry activated during refresh cycles to compensate for temperature and voltage drift
- Delay lines to support per-bit deskew

## DFT Implementation

The Combo PHY IP for Storage supports transition fault testing of the digital logic at-speed, with a second pass at the lower frequency to target the faults in the configurable delay lines. An additional test mode has been introduced in the DLL PHY scan implementation for this purpose.

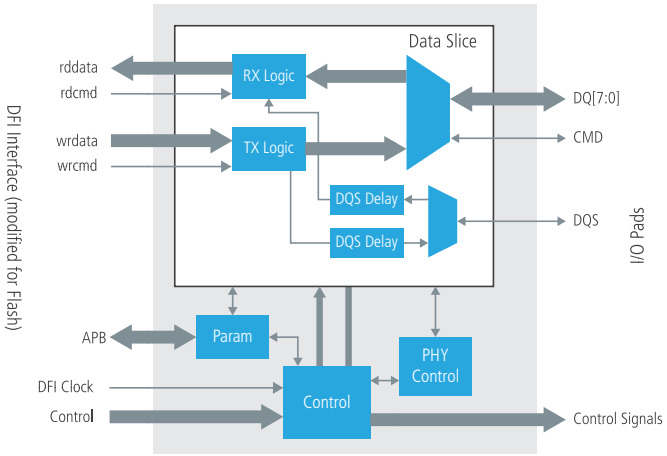


*Figure 2: IP-Level Block Diagram*

## Loopback Mode

The Combo PHY IP for Storage contains logic that allows for at-speed testing and data eye training without adding additional test multiplexers in critical timing paths in the design. The loopback testing mechanism includes a vector generation unit, which creates patterns for the write data path and then tracks the data back through the read data path. Internal loopback testing can be used during production to verify that critical logic, such as the DLL, write path, and read path, are functioning correctly. External loopback can be used to test the at-speed connectivity of the I/O pads.

## Protocol and Speed Support

The Combo PHY IP for Storage supports the following protocols:

| Protocol | Clock |
|---|---|
| ONFI 4.1, 4, 3, 2, 1, Toggle 2,1, Async | 600MHz |
| SD (legacy/UHS-I) | 200MHz |
| eMMC5.1 | 200MHz |
| xSPI | 200MHz |

## Deliverables

- Clean, readable, synthesizable Verilog RTL
- Synthesis and STA scripts
- Documentation including integration and user guide, release notes
- Verilog testbench with memory model, configuration files, and sample tests
- Verilog models of dummy I/O pads

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