

Host Controller IP for xSPI

Overview

With growing demand for flash memory in automotive, IoT, and consumer applications, as well as ever higher transfer rates and lower latency, the Cadence® Host Controller IP for xSPI offers up to 8 flash Serial Peripheral Interfaces (i.e., Octal SPI, HyperFlash, xSPI) to further increase the Serial Flash Memory throughput while providing backwards compatibility with single, dual, and quad I/O interfaces.

The Host Controller IP for xSPI supports Serial Flash devices that comply to the following standards:

- JEDEC xSPI (JESD251) v1.0
- JESD216C rev. 0.6
- Octal SPI – manufactured by Micron and Macronix
- HyperFlash – manufactured by Cypress
- QSPI – multiple vendors supported

The Host Controller IP for xSPI connects to a system-on-chip (SoC) host through Arm® AMBA® AXI buses for data interfaces (Slave and Master) and APB bus for the register interface.

The integrated soft combo PHY enables the highest speed clock rates, eliminating the need to generate a reference clock based on the Flash memory clock.

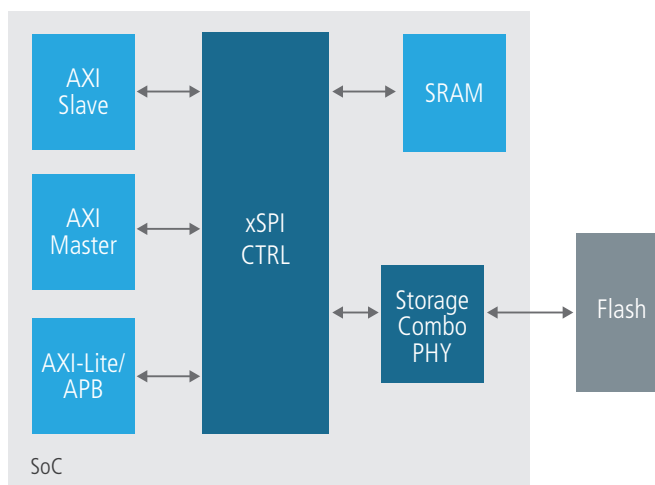


Figure 1: Example System-Level Block Diagram

Benefits

- Flexibility—Multiple SPI protocol support within single IP
- Simplicity—Using soft Storage Combo PHY IP simplifies SoC timing
- High performance—Supports maximum Octal SPI data rates and XIP (Execute In Place)

Key Features

- Support for multi CMD channels
- Supports JEDEC SFDP (Serial Function Discoverable Parameters)
- Memory mapped – enables BOOT and XIP functionality
- System interfaces: AXI, AXI-Lite, and APB
- DMA support for high-speed transfers
- All-digital storage combo PHY IP allows for accurate data sampling training and eliminates the need for high-speed clock for SPI interface
- Slave DMA interface directly to data buffer

Product Details

The Host Controller for xSPI is a complete solution supporting multiple SPI standards. It's compatible with devices from leading vendors, to ensure high versatility. The industry-standard AXI, AXI-Lite, and APB interfaces are supported to enable plug-and-play integration with most SoCs. The Host Controller for xSPI leverages the experience gained in development of multiple other Cadence Storage IP products.

Auto Command Engine

This module implements high-level JESD216 protocol functionality and multi-thread logic. It translates high-level commands into the series of low-level commands sent to the xSPI interface. This module has an embedded protocol engine that selects the most appropriate set of features of the chosen xSPI device, relieving the software engineer from the need to know low-level protocol details.

DMA Master

This module is used to automatically transfer data from the Host Controller IP for xSPI internal buffer to the system memory.

Generic Command Engine

This module provides low-level access to the xSPI interface, allowing the host to control each single operation triggered.

DMA Slave

This module provides high-performance slave interface to the controller's internal data buffer.

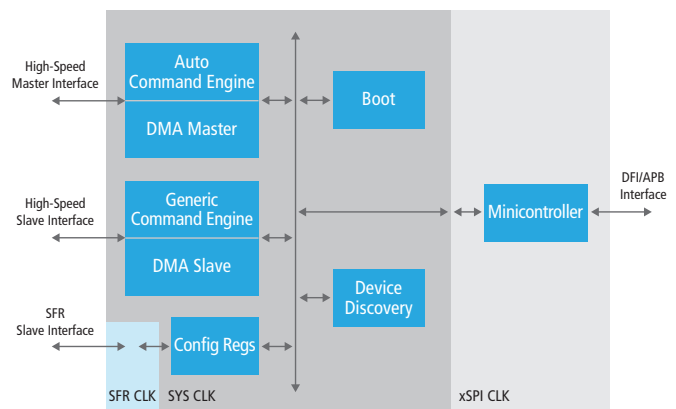


Figure 2: IP-Level Block Diagram

Boot

This module implements booting from the xSPI memory functionality.

Device Discovery

This module is used to identify memory device and pre-configure special function registers.

Minicontroller

This module gets a command stream and translates it into the physical operation on the xSPI interface using a PHY module. Additionally, the Minicontroller module regulates data flow between the physical xSPI interface and the system interface.

Related Products

- Cadence Storage Combo PHY IP
- Cadence NAND Flash Controller IP

Deliverables

- Clean, readable, synthesizable Verilog RTL
- Verilog testbench with memory model, configuration files, and sample tests
- Cadence Genus® Synthesis Solution scripts
- Documentation—integration and user guide, release notes
- Top layer for integration

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