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Design IP Datasheet

Denali Gen2 DDR PHY IP for LPDDR5/4/4x for TSMC 7 FinFET Process

Overview

Today's consumers generate and consume large volumes of data and video, exploding the need for data-intensive processing requiring high memory bandwidth. The Cadence® Denali® Gen2 DDR PHY IP for LPDDR5/4/4x for TSMC 7 FinFET Process is a family of high-speed on-chip interfaces to external memories supporting these high-performance requirements with products that are optimized for each application's needs.

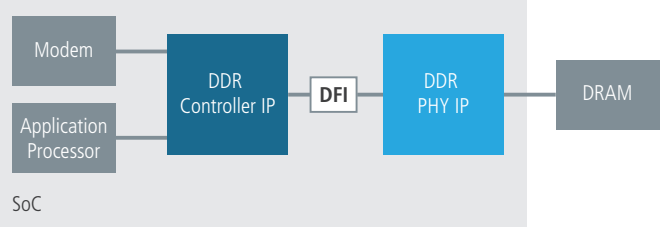

Figure 1: Example System-Level Block Diagram

The Denali Gen2 High-Speed DDR PHY IP is comprised of architectural improvements to its highly successful predecessor, achieving breakthrough performance, lower power consumption, and smaller overall area. The application-optimized DDR PHY IP can achieve speeds up to 5400Mbps. Low-power features include the addition of a VDD low-power idle state in the PHY and power-efficient clocking during low-speed operation for longer battery life and greener operation. Redesigned I/O elements reduce overall area by up to 20%.

Benefits

- **Lowest latency for data-intensive applications**
- **Highest data rates with detailed system guidelines**
- **Maximum system margin with advanced clocking and I/O architectures while reducing power and area**

The DDR PHY IP is developed by experienced teams with industry-leading domain expertise and extensively validated with multiple hardware platforms. It is engineered to quickly and easily integrate into an SoC, and is verified with the Denali Controller IP for DDR as part of a complete memory subsystem solution. The DDR PHY IP is designed to connect seamlessly and work with a third-party DFI-compliant memory controller.

Key Features

- Application-optimized configurations for fast time to delivery and lower risk
- Low-power VDD idle, VDD light sleep, and power-efficient clocking in low-speed modes
- Memory controller interface complies with DFI5.0 standard
- I/O pads with impedance calibration logic and data retention capability
- Internal and external datapath loop-back modes
- RX and TX equalization for heavily loaded systems
- Per-bit deskew on read and write datapath
- Fine-grain custom delay cell for delay tuning

Product Details

The DDR PHY IP consists of a DFI interface to the memory controller, external register interface (configuration and test), PHY control block (initialization and calibration logic), and configurable data slices.

The DDR PHY IP is a high-performance DQS-delay architecture that uses programmable clock delay lines to align write data, read data capture, and DQS gating from the I/O pads across the DFI interface to the memory controller.

PHY Architecture

To optimize the DDR interface implementation, the DDR PHY IP provides complete flexibility with process, library, floorplan, I/O pitch, packaging, metal stack up, routing, and other physical parameters.

The DDR PHY IP is implemented with a slice-based architecture that supports a wide range of memory classes and data rates.

Data Slice and Address/Control Slices

The data slice is an 8-bit-wide design that interfaces to the DQ, DM, and DQS connections of the DRAM. The data slice is duplicated to create the appropriate data width, allowing flexibility to adjust to meet the requirements of the systems or applications.

The Address and Address/Control slices interface to the control, command, and address connections of the DRAM. The Address or Address/Control slice is duplicated to create the appropriate width for different protocols or combination of protocols, allowing flexibility to adjust the number of control, command, and address signals as needed.

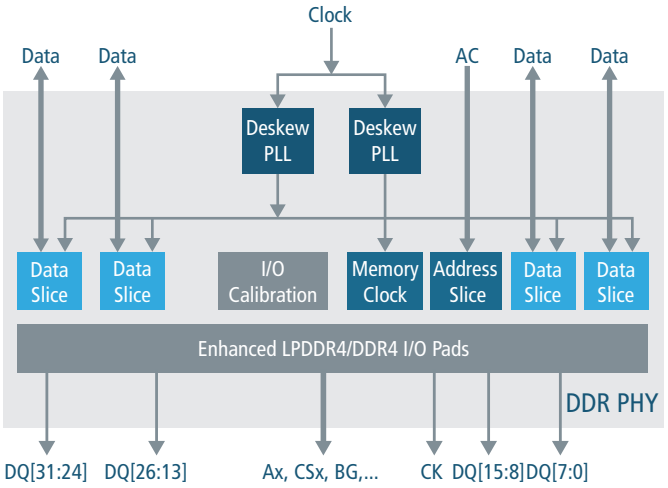

Figure 2: IP-Level Block Diagram

External Register Interface

The external register interface is a Cadence-proprietary interface to access the data slice registers.

PHY Control Block

The DDR PHY IP control block provides initialization and calibration logic for training the DQS alignment for each data slice.

Availability

The DDR PHY IP is available with various configurations and supports the following protocols:

Protocol	Speed	Process node
LPDDR5/4X/4	HS-5400	TSMC 7 FinFET

Related Products

- Cadence Denali Controller IP for LPDDR4x/4

Deliverables

- GDS II macros with abstract in LEF
- Verilog post-layout netlist
- STA scripts for use at chip or standalone PHY levels
- Liberty timing model
- SDF for back-annotated timing verification
- Verilog models of I/O pads, and RTL for all PHY modules
- Verilog testbench with memory model, configuration files, and sample tests
- Documentation: integration and user guide, release notes
- Verification IP setup files
- IBIS models

For more information, visit ip.cadence.com

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