112Gbps Long-Reach SerDes IP for TSMC 7nm

Overview

The Cadence® 112Gbps Long-Reach SerDes IP for TSMC 7nm operates at a full-rate of 112Gbps using PAM-4 modulation and half-rate of 56Gbps using PAM-4 modulation, as well as 56/28/10Gbps using NRZ. This IP enables high-speed communications between chips, backplane, and long-haul optical interconnects by converting between parallel data and extremely high-speed serial data streams with improved signal reliability. The area- and power-optimized design is ideal for high port-density applications that require long-reach and medium-reach links.

The 112G SerDes IP supports true plesiochronous operation at the data rates listed in Table 1 within +/- 200ppm. An integrated microcontroller allows for fully autonomous startup, adaptation, and service operation without requiring ASIC intervention. A programming and observation interface is provided via a parallel bus with MDIO-style addressing (port, device, address).

There are several comprehensive on-chip diagnostic tools that enable testability and easy debugging. A post-equalized histogram is available for accurate estimation of bit error rate (BER) even in the absence of actual bit errors. Vertical eye statistics can be logged to allow optional optimization of the device settings. The channel estimation hardware allows the accurate measurement of the channel response to assess package, connector, and trace characteristics.

Table 1. Transceiver operating data rates

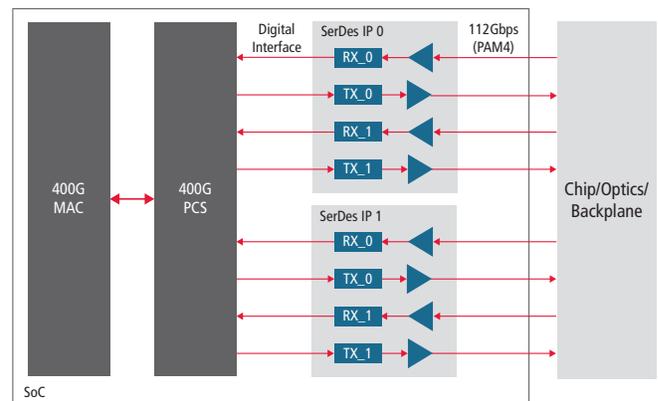|	
PAM-4 full-rate	103.125Gbps, 106.25Gbps
PAM-4 half-rate	51.5625Gbps, 53.125Gbps
NRZ full-rate	51.5625Gbps, 53.125Gbps
NRZ half-rate	25.78125Gbps, 26.5625 Gbps
NRZ 10G	10.3125Gbps

Figure 1: Example System-Level Block Diagram

Features

- TSMC 7nm FinFET CMOS Process
- 112/56Gbps PAM-4 or 56/28/10Gbps NRZ data rates
- Power-optimized for LR and MR links
- Compact footprint for high-density designs
- Fully autonomous startup and adaptation without requiring ASIC intervention
- Integrated BIST capable of producing and checking PRBS

Benefits

- **Best-in-class DSP supports long-reach lossy channels**
- **Small area and low power is ideal for high port-density applications**
- **Symmetric floorplan allows north-south and east-west SoC orientation**
- **Comprehensive on-chip diagnostic features make system testing/debugging quick and easy**

Product Details

There are two instances of the transmitter and the receiver in the IP.

Transmitter

The transmitter (TX) includes standard encoding, a DAC (microcontroller auto-calibrated) that converts digital signals to an analog output, with a digital FIR filter for waveform pre-emphasis. The transmitter drives a 100Ω differential output with adjustable swing.

Receiver

The receiver (RX) includes an analog front-end, an ADC (microcontroller auto-calibrated) that converts the analog input to digital signals, a DSP equalizer, and standard decoding.

Built-In Self Test (BIST)

The TX may be configured to transmit data from an internal PRBS generator using a list of selectable patterns. The RX may similarly be configured to deliver decoded bits to an internal self-synchronizing PRBS checker to count bit errors in the data stream. Received data may be looped back to the transmitter (see Figure 1).

Clocking and Reference Clocks

All timing is derived from an external 156.25MHz timing reference via an internal PLL and separate phase interpolators for the TX and RX lanes. The RX timing is locked to the incoming data, while the TX timing reference may be configured to derive either from the 156.25MHz external reference, or optionally from the RX timing.
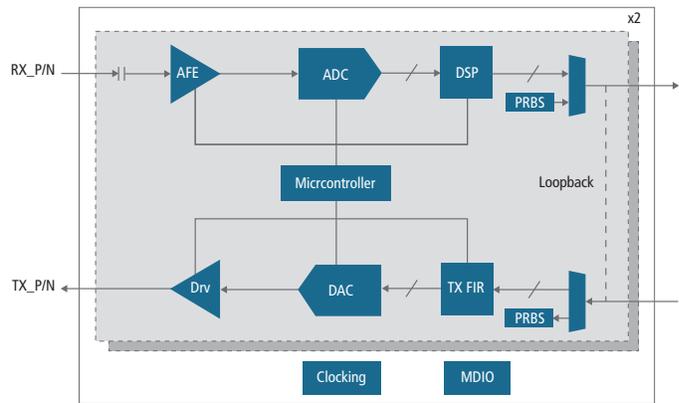

Figure 2: IP-Level Block Diagram

Related Products

- 10G/25G/50G/100G MAC

Deliverables

- GDS II macros with abstract in LEF
- Verilog post-layout netlist
- STA scripts for use at chip or standalone PHY levels
- Liberty timing model
- SDF for back-annotated timing verification
- Verilog models of I/O pads, and RTL for all PHY modules
- Verilog testbench with memory model, configuration files, and sample tests
- Documentation, including integration and user guide, release notes
- Verification IP setup files

For more information, visit ip.cadence.com