Design IP Datasheet

PHY IP for PCIe 3.0 for UMC 28HPC+

Overview

Modern applications demand lower latency and higher data transfer rates. Graphics cards, network interface cards (NICs), and storage accelerator devices need the bandwidth to deliver stunning visuals and high speed. The PCI Express® (PCIe®) protocol that makes these qualities possible needs an IP that is easy to use and provides a wide variety of configuration support.

The Cadence® PHY IP for PCIe 3.0 for UMC 28HPC is a hard PHY macro consisting of a Physical Media Attachment (PMA) layer and a soft Physical Coding Sublayer (PCS).

The PHY IP is designed to the PCIe 3.0 specification, and operates at 8.0GTps, 5.0GTps, and 2.5GTps. The PCS complies with the PIPE 3.0 and PIPE 4.2 specifications and provides support for the dynamic equalization features of PCIe 3.0. Cadence design-in kits provide flexibility in board design.

The PHY IP is architected to quickly and easily integrate into any system on chip (SoC), and to connect seamlessly to a Cadence or third-party PIPE 3.0-compliant or PIPE 4.2-compliant controller. Implemented on the UMC 28HPC+ processes, the PHY IP provides a cost-effective, low-power solution for demanding applications. It offers SoC integrators the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs.

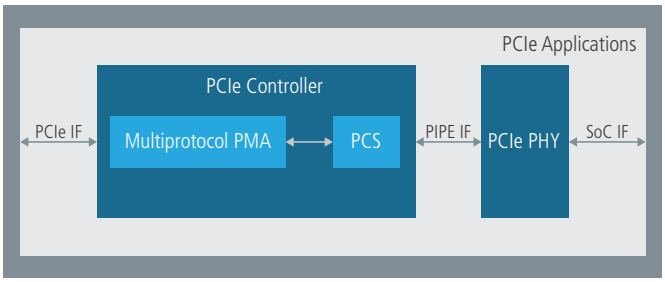

Figure 1: Example system-level block diagram

Benefits

- **Low-risk solutions— Hardened and silicon-proven design**
- **Extensive testability—BIST, Loop back, Scan feature with JTAG, and AMBA support**
- **Ease-of-use—System integration kit reduces system integration and signal integrity issues**

The PHY IP is silicon proven with extensive validation procedures to ensure a high-quality solution.

The PHY IP is part of the comprehensive Cadence Design IP portfolio comprised of interface, Denali® memory interface, analog, and systems and peripherals IP.

Key Features

- BIST for manufacturing test including loopback and pattern generator, error detector, and error counter
- On-chip regulation for high jitter performance
- Automatic calibration of analog circuits and offset correction
- Fully adaptive, continuous-time, linear equalizer
- APB, JTAG, and test mode interfaces for flexibility and ease of use
- Programmable 3-tap transmitter FIR with polarity inversion

Product Details

The PHY IP is a hard PHY macro for UMC 28HPC+ processes. I/O pads and ESD structures are included and this high-performance PCIe 3.0 design comes with L1 sub-states for low-power and green applications. The PHY IP supports PCIe 3.0, PCIe 2.1, and PCIe 1.1 specifications at speeds up to 8GTps. It is designed to easily integrate with a Cadence controller for PCIe, or any third-party controller with a PIPE 4.2-compliant interface.

PHY Architecture

The PHY IP is designed with a lane-based architecture, providing greater control over floorplanning, placement, packaging, and I/O integration than other hard PHY solutions, while maintaining the reliability and ease of use associated with GDSII macros. Delivered as a hardened PHY with I/Os connected, the PHY IP offers all the time-to-market advantages and proven design quality of traditional hard PHY designs while retaining flexibility.

With 10+ years of experience and 400+ successful designs in process nodes ranging from 180nm to 16nm, Cadence IP has been proven in everything from low-power MP3 players to leading-edge supercomputers. As an active member of the PCI-SIG organization, Cadence has early insight into emerging standards, and can quickly and easily adapt to critical and important changes to current standards.

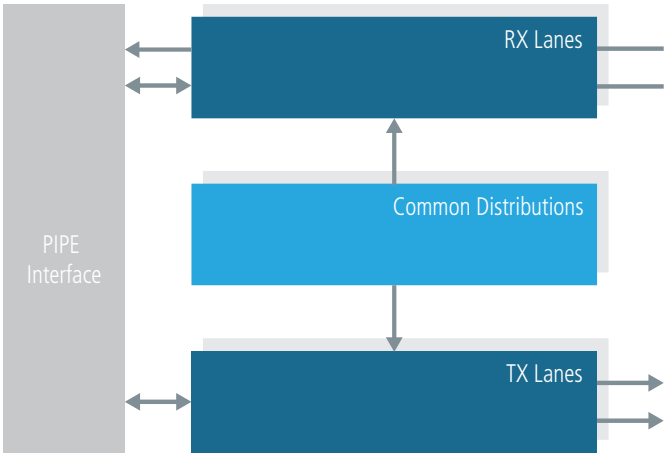

Figure 2: IP-level block diagram

Availability

The PHY IP is available with various configurations and supports the following protocols:

Protocol	Process node
PCIe 1.0, 2.0, and 3.0	UMC 28HPC+

Related Products

- Controller IP for PCIe 3.0
- PHY IP for PCIe 2.0

Deliverables

- Standard integration views: timing, physical views, LEF, DRC, LVS, ANT
- GDSII layout (optional)
- Liberty Timing model
- STA scripts
- Verilog model
- Verilog testbench and sample test cases
- Complete documentation customized to customer's specific configuration

For more information, visit ip.cadence.com

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