

IP for UFS 2.1 Host Controller

Overview

The Cadence® IP for the UFS 2.1 Host Controller is compliant with the UFS Architecture Specification (UFS), version 2.1, and the UFS Host Controller Specification (UFSHCI), version 2.1.

The IP for UFS 2.1 Host Controller is a standard-based serial interface for interfacing with a UFS storage device. The IP for UFS 2.1 Host Controller includes an integrated MIPI® UniProSM 1.6 protocol stack. The combined UFS and UniPro Controller integrates with MIPI M-PHYSM using a 20-bit or 40-bit RMMI interface.

The IP for UFS 2.1 Host Controller is architected to quickly and easily integrate into any system-on-chip (SoC) by using an AXI fabric. See Figure 1 for system-level block diagram.

A highly-efficient, cost-effective, and low-power solution, the IP for UFS 2.1 Host Controller contains a chaining DMA engine to reduce both the interrupt load on the application processor and the total system bus bandwidth requirement. Moreover, the buffer memory requirement within the core is minimized by transferring the data to system memory at physical interconnect rates.

The IP for UFS 2.1 Host Controller allows for highly-secured applications by employing AES encryption. The data encryption and decryption is done seamlessly by the controller as data is written to or read from the UFS 2.1 device.

Designed to meet safety-related automotive requirements according to ISO 26262, the IP for UFS 2.1 Host Controller is ASIL-B Ready and currently in use by several SoC designs for automotive and mobile applications.

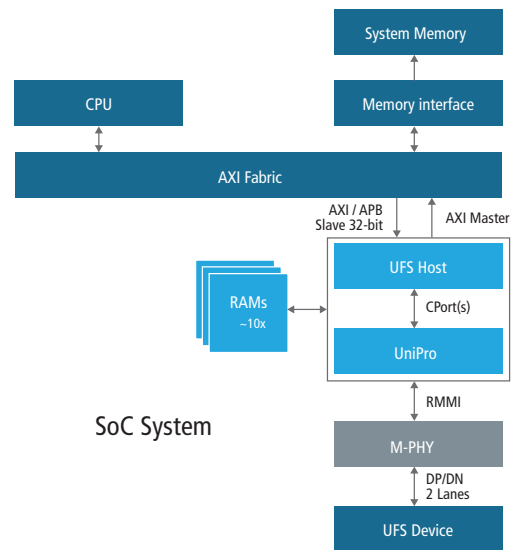


Figure 1: Example System-Level Block Diagram

Benefits

- **Layered software architecture controls all aspects of a UFS link**
- **Low-power—Power enables signals generated to control power shutdown of individual lanes**
- **Easy integration—Supports standard interfaces to other applications running on the SoC system**

Key Features

- Compliant with reference specifications for UFSHCI, UFS, and UniPro
- Support for the full range of UPIU packets, from 32 bytes up to 64KB
- SCSI commands executed without system host intervention after setup
- 32-bit APB or AXI Slave interface for system host programming access
- AES encryption for enhanced security
- AXI Master interface for fast data transfers

Product Details

The IP for UFS 2.1 Host Controller is a high-performance serial interface targeted primarily for automotive and mobile systems where data is stored on non-volatile mass-storage memory devices.

UFS Bus Master Transport Layer

This layer interprets inbound UMPIU packets and assembles outbound UMPIU packets. In contrast to the UFS Transport Protocol layer, the UFS Bus Master Transport layer supports requests from the UFS device to the IP for UFS 2.1 Host Controller.

Device Bus Master Manager

The device bus master manager contains a DMA engine, which has direct access to the system bus without going through the application layer. The benefits are that the UM operation is transparent to the application layer and hence the additional software impact and load on the system host are minimized. The DMA engine is directly controlled by the UFS device and hence shall be considered as a property of the device.

Service Access Points

There are several service access points used by the design, including inter alia UBM_SAP and UBM_UIC_SAP. The UBM_SAP service access point is used for communication between the device bus master manager and the UFS bus master transport layer, while UBM_UIC_SAP is responsible for communication between the UFS bus master transport layer and the UFS interconnect layer.

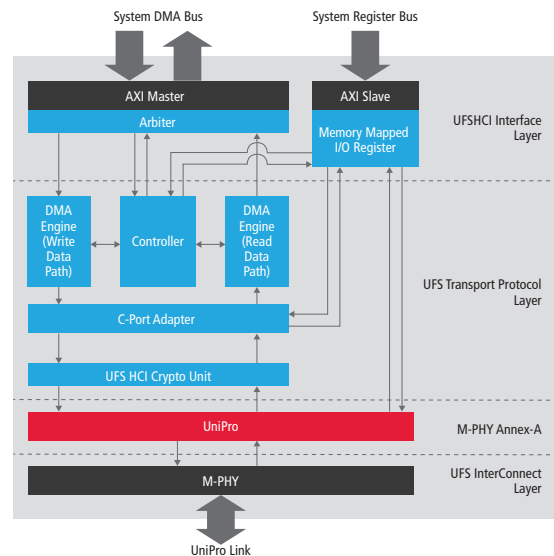


Figure 2: IP Architecture Overview

Functional Safety Features and Documentation

The IP for UFS 2.1 Host Controller has additional functional safety features targeting automotive applications. These features—including fatal fault detection, reporting, and recovery mechanisms—allow the IP for UFS 2.1 Host Controller to be capable of obtaining an ASIL-B Ready status without a need for many external diagnostic mechanisms. In addition to a safety manual, the deliverables also include a FMEDA report based on a representative design configuration.

Available Products

- Cadence IP for UFS 2.1 Host Controller

Related Products

- Cadence IP for MIPI M-PHY

Deliverables

- Ready to use, synthesizable IP for Verilog HDL
- Fully synchronous, synthesizable RTL
- Synthesis scripts and constraints
- Documentation including integration and user guide, release notes

For more information, visit ip.cadence.com



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