

# Simulation VIP for Bluetooth Low Energy

## Overview

Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

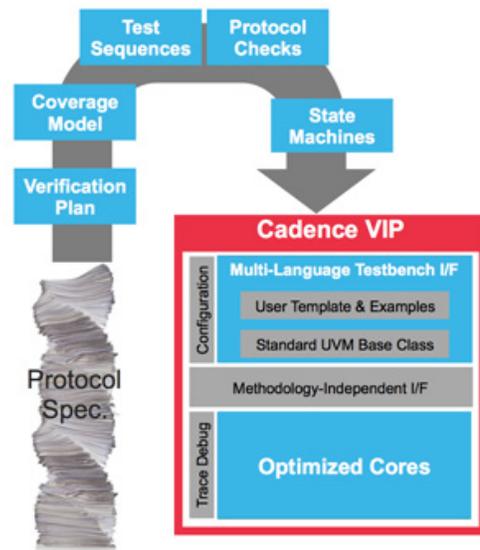
The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.

## Specification Support

The BLE VIP supports Bluetooth Specification version 4.2 and 5.0 available at <http://www.bluetooth.com>.

## Supported Design-Under-Test Configurations

- Controller     PHY     Controller + PHY
- Host



## Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification.

---

## Key Features

- High Duty, Low Duty, Directed, Undirected, Connectable, Non-connectable Advertisement.
- Support for all Control Procedures. For example, Connection Update and PHY Update.
- LL Privacy: Generation of Resolvable Private Address.
- LE Encryption: Counter with Cipher Block Chaining-Message Authentication Code (CCM) Mode
- LE Host Controller Interface commands/events/data fully supported.
- UART/USB/User-Defined protocol as a HCI transport layer.
- 2 Mbps/s packets transmission and reception capability.
- LE Long Range: Configurable Coded PHY for FEC (2-Block) with S=2/S=8.
- LE Advertising Extensions: Advertisement/Connection on Primary/Secondary Channels using EXT/AUX PDUs, Periodic Advertisement.
- LE Channel Selection Algorithm#2: Counter based Channel Selection Algorithm for Secondary Channels.



Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today's electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today's mobile, cloud, and connectivity applications. [www.cadence.com](http://www.cadence.com)

© 2014 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence and the Cadence logo are registered trademarks of Cadence Design Systems, Inc. in the United States and other countries.