Design IP Brochure

25Gbps Multi-Link and Multi-Protocol PHY IP for TSMC 7nm FinFET

Overview

The Cadence® 25Gbps Multi-Link and Multi-Protocol PHY IP for TSMC 7nm is a high-performance SerDes operating from 1.25 to 25Gbps specifically designed for infrastructure and datacenter applications. It features long reach equalization capability at very low active and standby power. The SerDes offers very low latency for time critical application for enterprise-level data communications, networking, and storage systems.

The PHY IP provides extensive flexibility to mix and match protocols within the same macro. The PHY IP is designed to simultaneously run PCIe®, CCIX, USB, SATA, 10G-KR, XAUI/RXAUI, and SGMII on a per lane basis. Multiple test features are embedded and easily accessible by the end-user. A user-friendly graphical interface called EyeSurf™ provides convenient access to real-time and non-destructive eye scope and bathtubs for monitoring the bit error rate (BER) and the link performance during live traffic.

The PHY IP quickly and easily integrates into any system on chip (SoC), and connects seamlessly to a Cadence controller for full flexibility. This minimizes the time and risk of device development. It offers SoC integrators the advanced capabilities, flexibilities, and support for advanced, high-performance designs. This IP can be configured by Cadence to be a full Multi-Protocol PHY or a PHY that supports a subset of standards, where the different protocols can be ordered as options.

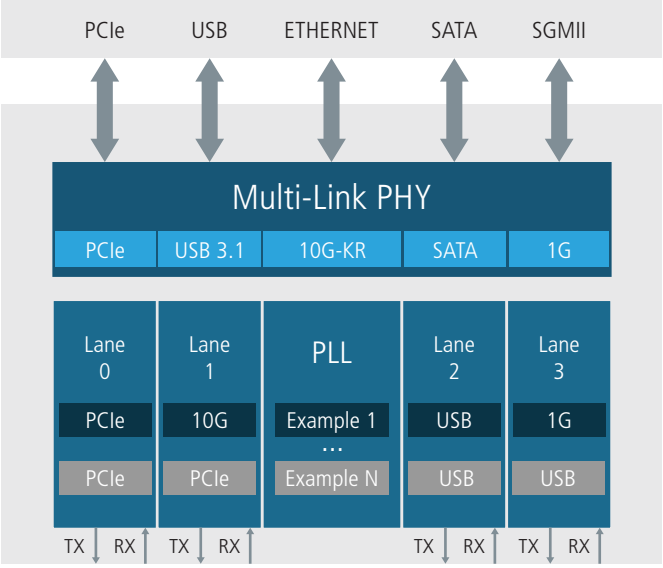

Figure 1: Example System-Level Block Diagram

Benefits

- Maturity – Silicon proven and robust Serdes architecture
- Flexibility – Maximum flexibility and reconfigurability
- Ease-of-use – Faster to integrate, bring-up, and support

Key Features

- High performance PHY for datacenter applications
- Low-latency, long reach and low power modes
- Wide range of protocols that support networking, storage and computing applications
- Multi-Link PHY—mix protocols within the same macro
- EyeSurf —non-destructive on-chip oscilloscope
- Extensive set of isolation, test modes and loop-backs including APB and JTAG
- Supports 16-bit, 20-bit, and 32-bit PIPE and non-PIPE interfaces
- Selectable serial pin polarity reversal for both transmit and receive paths

Product Details

The PHY IP provides performance, reliability, and robustness for the most demanding applications.

The PHY IP is architected as a hard PHY macro with a Physical Media Attachment (PMA) layer and a soft Physical Coding Sublayer (PCS) available for various processes. The PHY IP supports long reach (LR) backplane with insertion loss in excess of 30dB for rates up to 16G and medium reach (MR) with insertion loss up to 25dB for rates up to 25G. It is specifically optimized to minimize end-to-end latency, and power. Low power modes are also supported (ex. PCIe L1 substates, SATA slumber/partial, etc.) for energy efficient applications. For robustness the PHY is designed
to operate from -40 to 125 degrees C, it features superior ESD protection and it is designed to exceed the stringent reliability requirements of datacenter applications.

The PCS complies with the latest PCIe PIPE specification and provides support for the dynamic equalization features of different interface protocols. The PHY IP is designed for handling multi-protocols on one single PHY macro (see table below).

PHY Architecture

The PHY IP is designed with a multi-link lane-based architecture, providing greater control over floor planning, placement, packaging, and I/O integration than other hard PHY solutions, while maintaining reliability and ease of use associated with GDSII macros.

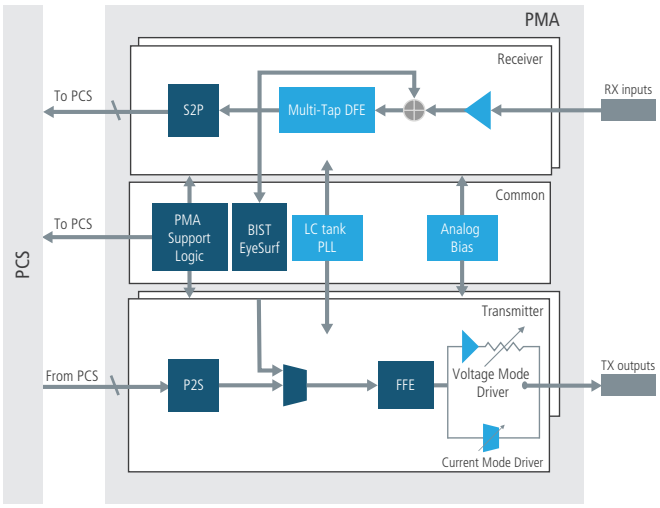

Figure 2: IP-Level Block Diagram

Availability

The PHY IP is available with various configurations and supports the following protocols:

Protocol*	Data Rate (Gbps/Lane)	Process node
CCIX	Up to 25	7nm FinFET
PCIe 4/3/2/1	Up to 16	7nm FinFET
USB 3.1 Gen 2 and Gen 1	10 and 5	7nm FinFET
10G-KR	10.3125	7nm FinFET
SATA 3/2/1	6	7nm FinFET
RXAUI/XAUI	6.25/2.5	7nm FinFET
QSGMII/SGMII	5/1.25	7nm FinFET

*Base product supports one protocol. Additional protocol support available as options.

Related Products

- Cadence Controller IP for Cache Coherent Interconnect for Accelerators (CCIX)
- Cadence Controller IP for PCIe 4.0, 3.0, 2.0, 1.0
- Cadence IP for Multi-Protocol PCS

Deliverables

- Integration Views—Verilog behavioral model, GDSII, CDL, and power models
- Synthesizable RTL
- DFT-Verilog netlists with SS/FF, CTL, and BSDL
- Reference Verilog testbenches used for generating SoC level VCD ATE test patterns for PHY
- IBIS-AMI kit
- Documentation—XML, integration and user guide, release notes
- Testboards available on demand

For more information, visit ip.cadence.com

cadence®

Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today's electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today's mobile, automotive, cloud, and connectivity applications. www.cadence.com