

Controller IP for Cache Coherent Interconnect for Accelerators (CCIX)

Overview

Today's data center throughput is constrained by limitations of computational speed and power consumption. In order to keep up with the growth in data and computational complexity, new approaches to accelerating applications are being explored. One such area of innovation is the acceleration of applications across multiple servers using shared data storage. The Cache Coherent Interconnect for Accelerators (CCIX), is a new chip-to-chip interconnect based on PCI Express® (PCIe®), that allows two or more devices to share data in a cache coherent manner running at speeds up to 25Gbps. CCIX allows processors in a heterogeneous computing architecture to extend their cache coherency to accelerators, interconnect, and I/O.

The Cadence® Controller IP for CCIX is built on top of our mature PCI Express solution that is widely deployed in multiple products in production. It provides shared data access significantly improving compute efficiency for servers running data center workloads. The Controller IP is engineered to quickly and easily integrate into any system-on-chip (SoC) and connect seamlessly to a Cadence or 3rd-party PIPE 4.x-compliant PHY.

The Controller IP is part of the comprehensive Cadence Design IP portfolio comprised of interface, Denali memory interface, analog, and systems and peripherals IP.

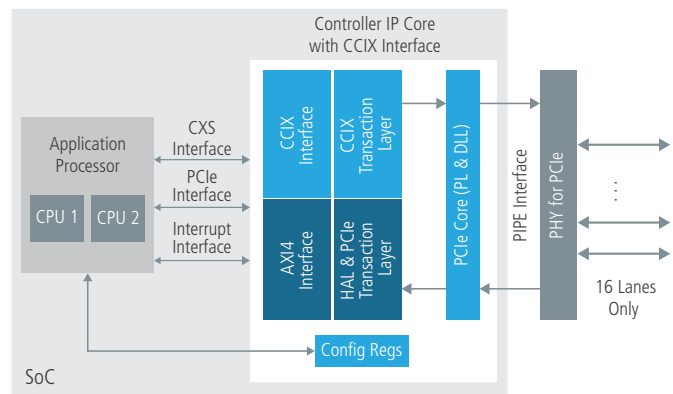


Figure 1: Example System-Level Block Diagram

Benefits

- **Faster system integration with pre-integrated PHY, Controller, drivers, and Verification IP**
- **Reduced risk from using silicon proven PCI Express 4.0 solution**
- **Higher quality from applying complete Cadence verification solution**

Key Features

- Optimized, tightly coupled interface between processors and accelerators
- Dedicated AXI™4 interface for priority traffic (QoS)
- Low latency interface
- Built on robust PCI Express 4.0 solution (can run in PCIe only mode) with CCIX specific transaction layer
- Support for Vendor Defined Messages (VDMs) and optimized Transition Layer Packets (TLPs)

Product Details

The Controller IP allows in-line bump in the wire acceleration for network packet processing, storage acceleration and off-line acceleration by using a co-processor model. It fits into existing PCI Express system architecture and leverages existing form factors. The controller has a dedicated interface for CCIX traffic and a AXI-4 interface for PCI Express traffic.

Controllers

The Controller IP is based on silicon-proven PCIe Controller supporting 16 lanes up to 16Gbps per lane. It leverages the existing PCIe 4.0 PHY, Data Link and Transaction Layers. There are three main blocks in a CCIX controller:

- PCI Express PHY and Data Link layer common for PCI Express and CCIX
- PCI Express 4.0 Transaction Layer and dedicated AXI-4 interface for PCIe traffic
- CCIX Transaction Layer and dedicated CCIX interface for CCIX traffic

Dedicated datapath for CCIX and independent VC allows the system to transmit CCIX traffic with the highest priority. The CCIX Transaction Layer supports Optimized Transaction Layer Packets for optimal efficiency.

PHYs

Cadence offers PCIe 4.0-based PHY IP, that supports data rates up to 25Gbps.

Software

The Controller IP comes with Core Firmware driver and Reference Linux driver. The firmware is OS independent and has a Local Management Interface (LMI) with hardware-specific registers.

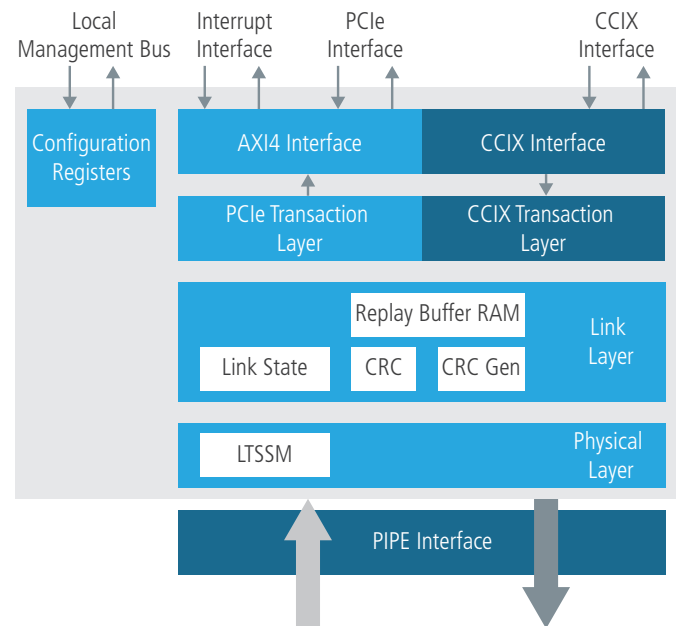


Figure 2: IP-Level Block Diagram

The firmware is tested with the Controller IP using Virtual Reference Platform (VSP). The Reference Linux driver is integrated in the OS wrapper. Functional Partition Driver consists of External Interrupt (ISR), Fabric Access and memory allocation. It can be modified based on the application.

Integrated solution

The Controller IP, PHY, Software and VIP are integrated and verified as a solution to reduce risk and improve time-to-market.

Availability

- Cadence Controller IP for CCIX

Related Products

- Cadence PHY IP for CCIX
- Cadence PHY IP for PCI Express 4.0
- Cadence Controller IP for PCI Express 4.0
- Cadence Integrated Solution for PCI Express 4.0
- Cadence Verification IP for CCIX

Deliverables

- Verilog HDL Source Code
- Testbench
- Cadence RTL compiler synthesis scripts
- Firmware Core Driver
- Documentation

For more information, visit ip.cadence.com

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