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VIP Datasheet

Simulation VIP for CCIX

For datacenter acceleration applications requiring cache coherency

Overview

The Cadence® verification IP (VIP) for Cache Coherent Interconnect for Accelerators (CCIX) is a member of Cadence's broad enterprise VIP portfolio. CCIX is an open standard for a new class of server products that addresses the challenging performance and latency requirements in the growing datacenter market.

The VIP for CCIX showcases Cadence's pioneering efforts in the enterprise datacenter market by being the first to announce a VIP-DIP solution. With early customer engagements prior to specification ratification and joint collaboration with Cadence DIP, this VIP allows customers to leverage our expertise in PCI Express® (PCIe®) and cache coherency from the verification and design spectrum.

Built on top of an industry-known and proven PCIe and ARM® AMBA® verification solutions, the VIP for CCIX runs on all simulators and supports SystemVerilog along with the widely adopted Universal Verification Methodology (UVM). This enables verification teams to reduce time spent on environment development, and redirect the saved time to cover a larger verification space, accelerate verification closure, and ensure end product quality.

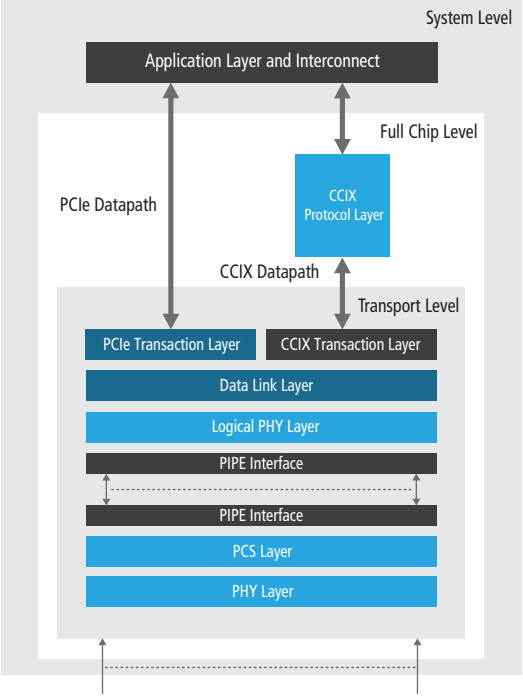

Figure 1: Example system-level block diagram

Specification Support

The simulation VIP for CCIX supports the CCIX specification.

Supported Design-Under-Test Configurations

☑ PCIe in CCIX mode (transport level)

☑ CCIX full stack (full chip)

☑ CXS standalone

☑ CCIX PRL over CXS

Benefits

- Ability to generate traffic and verify all CCIX interfaces
- Ability to generate and verify PCIe and CCIX packets in CCIX mode
- Layered architecture coupled with callbacks to enable verification of each functional layer

Key Verification Capabilities

The VIP for CCIX delivers:

- Full timing configurability
- Pre-programmed assertions that continuously watch simulation traffic to check for protocol violations
- Pre-programmed coverage models used to verify exercising of various modes of operation of an interface
- Pre defined and user-defined error injection capability available at each protocol layer

Key Features

- PCIe traffic with support for CCIX mode
- Configurable to transmit PCIe packets, as well as CCIX packets
- Supports TX and RX channels simultaneously
- 16G speed support
- Dedicated VC to CCIX traffic that can be configured to:
  - Send vendor-defined messages with CCIX payload
  - Send/receive CCIX-optimized TLP
- Supports transmission and reception of vendor-defined messages and optimized messages
- Provides support for PIPE 4.3 and serial interfaces
- Supports up to 1024 flit width
- Interconnect monitor for cache-coherent automatic checking
- Ability to pack/unpack coherent transaction to CCIX messages and send/receive them over PCIe
- Protocol checks and assertions
- Protocol activation signals

Supported Tools

- Interconnect Workbench
- Interconnect Validator

Related Products

- Cadence VIP for PCIe Gen4
- Cadence VIP for AMBA Protocols
- Cadence Controller IP for CCIX

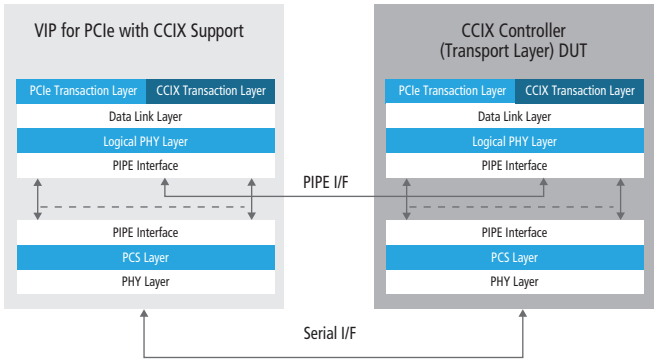

Figure 2: CCIX transport layer verification at PIPE or serial interface

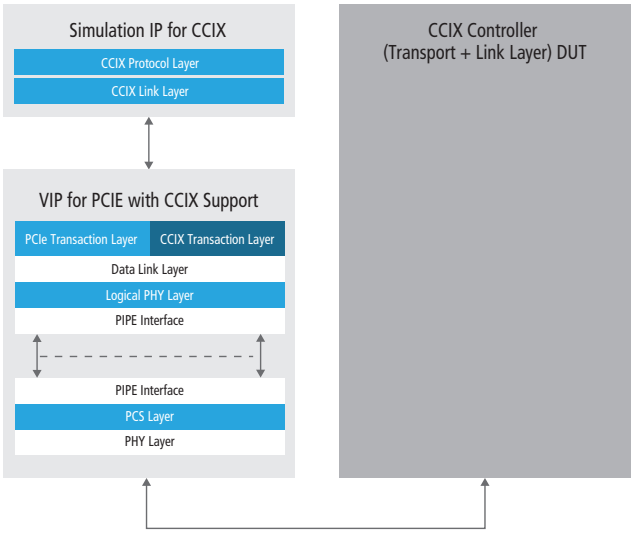

Figure 3: CCIX full stack verification

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