

Simulation VIP for SAS 24G

For mission-critical enterprise storage subsystems

Overview

Cadence® Simulation Verification IP (VIP) is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

Cadence’s VIP for Serial Attached SCSI (SAS) 24G is the newest member to Cadence’s broad storage interface VIP for portfolio. SAS has been the interface of choice for mission-critical enterprise storage subsystems with the next-generation SAS 24G addressing the transmission and storage of data growing at an exponential rate due to an increasingly connected world.

Built on top of a pioneering, flexible architecture designed for performance and easy integration in testbenches at the IP, system-on-chip (SoC), and system level, the Simulation VIP for SAS 24G runs on all simulators and supports SystemVerilog along with the widely adopted Universal Verification Methodology (UVM). This enables verification teams to reduce time spent on environment development, and redirect the saved time to cover a larger verification space, accelerate verification closure, and ensure end product quality.

Specification Support

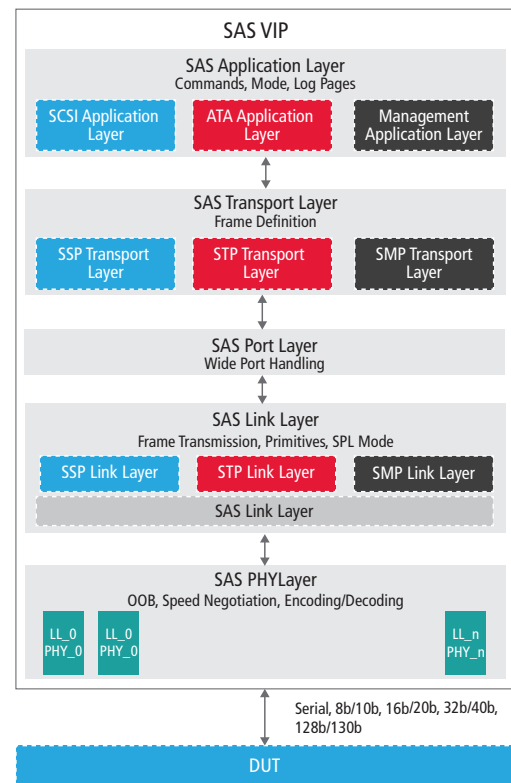
The Simulation VIP for SAS 24G supports SAS Protocol Layer (SPL) 4.

Benefits

- Ability to generate and verify traffic at all SAS generation data rates for DWORD and packet mode (1.5G, 3G, 6G, 12G, and 24G)
- Ability to verify all SAS device configurations (initiator, target, and expander)
- Layered architecture coupled with callbacks to enable verification of each functional layer

Supported Design-Under-Test Configurations

- Initiator
- Target
- Expander



Simulation VIP for SAS 24G layered architecture coupled with callbacks enables verification of each functional layer

Key Verification Capabilities

The Simulation VIP for SAS 24G delivers

- Complete Active and Passive State machine models incorporating support for power-saving modes
- Full timing configurability
- Pre-programmed assertions that continuously watch simulation traffic to check for protocol violations
- Pre-programmed coverage models used to verify exercising of various modes of operation of an interface
- Predefined and user-defined error injection capability available at each protocol layer

Key Features

- Supports Initiator, Target, Expander (edge and fanout)
- Supports all SAS speeds: 1.5, 3, 6, 12, 24 Gb/s
 - DWORD mode: 12Gb/s and lower
 - Packet mode: 24Gb/s and greater
- Configurable interface support for serial and parallel interfaces for DWORD and packet modes
 - DWORD modes: serial, 8b/10b, 16b/20b, 32b/40b
 - Packet modes: serial (including FEC), 128b/130b
- Supports narrow and wide ports
 - Narrow: One PHY in port
 - Wide: Greater than one PHY per port
- Supports OOB sequence, speed negotiation sequence generation, and verification at all data rates
- Supports active PHY transmitter adjustment (APTA) in packet mode
- Supports persistent connection in SSP connection
- Supports complete set of primitives (generation and verification)
- Supports multiplexing of logical links
- Supports all broadcast types
- Support all frames (generation and verification)
- Supports OOB, speed negotiation, and training bypass capabilities

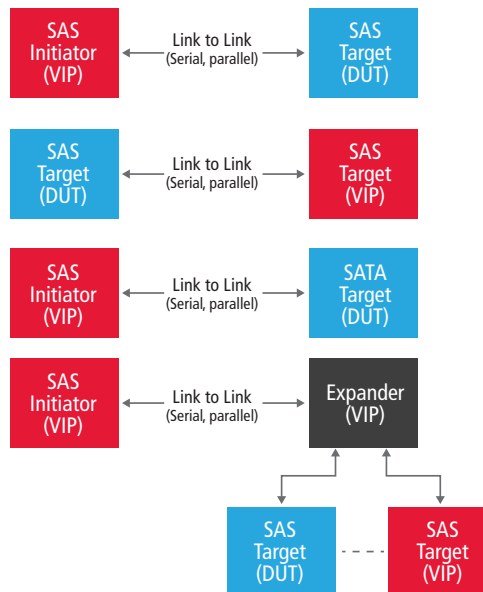
Supported Tools

The Simulation VIP for SAS 24G includes a basic test suite capability.

Related Products - Cadence

- Cadence Simulation VIP for NVM Express
- Cadence Simulation VIP for SATA

Supported Configurations



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