

I2C High-Speed Bus Controller (I2C-HS) IP

Overview

Cadence® IP Factory delivers custom, synthesizable IP to support specific design requirements.

The **Cadence I2C High-Speed Bus Controller IP** is compliant with Philips *I²C-Bus Specification* version 2.1 and *AMBA® 2 Specification*.

The **Cadence I2C High-Speed Bus Controller IP** is a microcode-free design targeted at ASIC and FPGA implementations. Supporting a completely synchronous architecture, positive-edge clocking, and no internal wait states, scan insertion is straightforward.

The **Cadence I2C High-Speed Bus Controller IP** is architected to quickly and easily integrate into any system on chip (SoC) that supports an ARM® AMBA® 2 Advanced Peripheral Bus (APB), and to connect seamlessly to Cadence, or third-party, APB-based bus master devices, and I²C devices at speeds up to 3.4Mbps.

The **Cadence I2C High-Speed Bus Controller IP** provides a convenient, cost-effective connection between your SoC and external I²C devices. It offers SoC integrators the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs and implementations.

Cadence SoC Peripheral IP is silicon proven and has been extensively validated with multiple hardware platforms.

Cadence IP Factory offers comprehensive IP solutions that are in volume production, and have been successfully implemented in more than 400 applications.

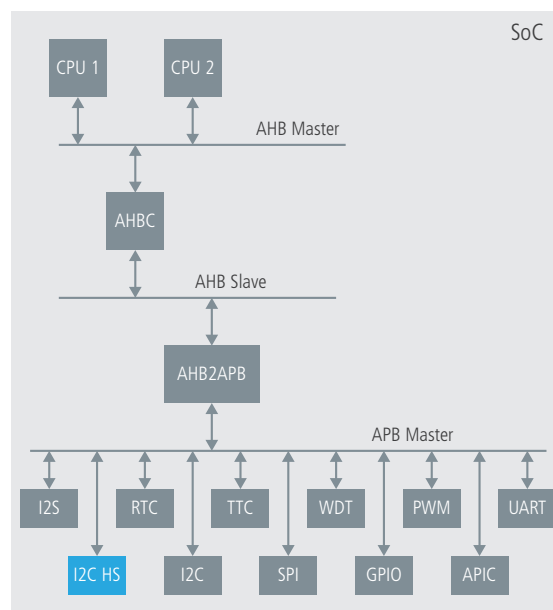


Figure 1: Example System-level Block Diagram

Key Features

- Compliant with I²C Specification v2.1
- Supports standard (up to 100Kbps), fast (up to 400Kbps), and high-speed (up to 3.4Mbps) modes
- Supports 7- and 10-bit slave addresses
- APB slave interface to SoC
- Master, master memory, multimaster, and slave operating modes supported in both RX and TX
- Runtime slave address selection

Product Details

The **Cadence I2C High-Speed Bus Controller IP** interfaces CPU cores and other on-chip APB-based bus master devices to a broad range of off-chip I2C peripherals.

I2C Bus Interface

The I2C Bus Interface module handles all bit operations directly at the I2C bus level, freeing the application processor for other tasks while I2C communication is ongoing. In slave mode, the I2C Bus Interface module detects start and stop conditions, acknowledge, operation direction, etc. In master mode, it controls the state of SCL and SDA according to requests from the host application.

Control Logic

The control logic module handles all byte-level formatting required for compliance with the I2C bus protocol.

Signal Interfaces

The **Cadence I2C High-Speed Bus Controller IP** supports an APB slave interface for connection to APB-based bus masters such as a CPU core, or AHB2APB bridge. The APB slave interface includes PSEL and PENABLE, allowing a single SoC to contain multiple **Cadence I2C High-Speed Bus Controller IP**.

Serial Clock Generator

The serial clock generator is a programmable divider that provides the I2C clock signal (SCL) when the **Cadence I2C High-Speed**

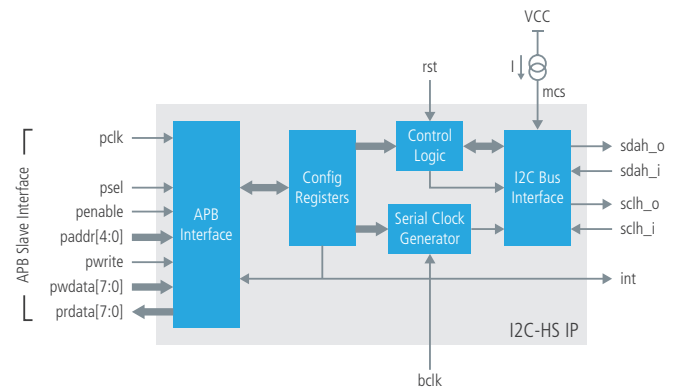


Figure 2: IP-level Block Diagram

Bus Controller IP is operating in any of the master modes. The clock source to the serial clock generator can be from the system clock, or an external clock input.

The serial clock generator is disabled when the **Cadence I2C High-Speed Bus Controller IP** is in slave mode.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of SoC Peripheral IP to meet your design requirements.

With 10+ years of experience and 400+ successful designs in process nodes ranging from 180nm to 22nm, **Cadence IP Factory** solutions have been proven in everything from low-power MP3 players to leading edge supercomputers.

For more information, visit ip.cadence.com

Benefits

- Low-risk solution—silicon-proven design
- Ease-of-use—customizable with easy integration
- Easy integration—supports industry-standard PSCI and APB interfaces

Related Products

- Inter Integrated Circuit (I2C) IP

Deliverables

- Clean, readable, synthesizable Verilog HDL
- Cadence Encounter® RTL Compiler synthesis scripts
- Documentation – integration and user guide, release notes
- Sample verification testbench

Available Products

- I2C High-Speed Bus Controller (I2C-HS) IP

cadence®

Cadence Design Systems enables global electronic design innovation and plays an essential role in the creation of today's electronics. Customers use Cadence software, hardware, IP, and expertise to design and verify today's mobile, cloud, and connectivity applications. www.cadence.com

© 2014 Cadence Design Systems, Inc. All rights reserved worldwide. Cadence, the Cadence logo, and Encounter are registered trademarks of Cadence Design Systems, Inc. in the United States and other countries. AMBA and ARM are registered trademarks of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. All rights reserved. APB is a trademark of ARM Limited (or its subsidiaries) in the EU and/or elsewhere. All other trademarks are the property of their respective owners.

V2.2 07/14