

# PHY IP for NAND Flash ONFI 4.1 / Toggle 2

## Overview

The Cadence® PHY IP for NAND Flash ONFI 4.1 / Toggle 2 is an all digital soft PHY with a DFI 3.0 interface optimized for NAND Flash. It also has a register interface for configuration and calibration of the PHY settings. The integration of the soft PHY enables the highest clock rates without the need for a faster (4X) reference clock, which in turn enables simplified SoC designs, reduced number of clock domains, and power savings. The PHY contains a per-bit deskew mechanism, which improves the data window for the highest speed modes.

The PHY IP supports all ONFI speed modes defined in the ONFI 4.1 specification, backwards compatible to all previous ONFI specifications. It also supports Toggle 1 and Toggle 2 interfaces, as well as legacy asynchronous interface. It is compatible with all major NAND devices.

The PHY IP is architected to quickly and easily integrate into any system on chip (SoC), and to connect seamlessly to the Cadence NAND Flash Controller IP or a third-party NAND Flash controller using the DFI 3.0 interface.

It offers SoC integrators the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs and implementations. The PHY IP supports speeds up to 600MHz and is structured so that future clock rate increases can be easily accommodated.

The PHY IP offers an automated design flow with advanced synthesis and static timing analysis (STA) scripts that permits RTL-to-placed gates in an easy manner.

Based on Cadence's own LPDDR3 PHY design, the PHY IP is silicon proven, and has been extensively validated with multiple hardware platforms.

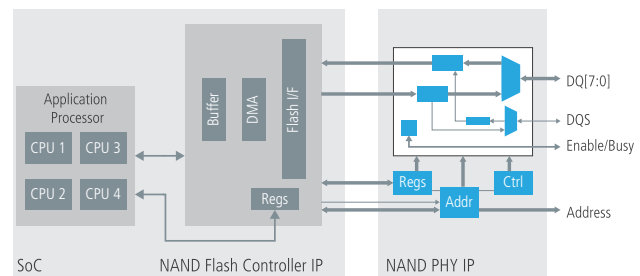


Figure 1: Example System-Level Block Diagram

## Benefits

- **Optimized for low power and small area**
- **Soft PHY for integration flexibility**
- **Low-risk and silicon-proven design**

## Key Features

- Integrated DLL supports speeds up to 600MHz
- Supports ONFI 1, 2, 3, 4, 4.1 and Toggle 1, 2 devices
- Includes per-bit deskew mechanism
- Fully digital soft PHY implementation
- DFI 3.0 interface optimized for NAND
- Register interface for PHY programming

## Product Details

The PHY IP is a single module that encapsulates all functionality required to interface to external NAND Flash devices. It is compatible with all major NAND Flash devices. The NAND Flash DLL PHY IP supports ONFI 4.1, 4, 3, 2, 1 and Toggle 2, 1 interfaces as well as legacy asynchronous devices. This module has a register interface for setup, configuration, and calibration of the ONFI bus.

The PHY IP is based on the proven Cadence LPDDR3 PHY IP design, widely deployed across a range of silicon nodes.

## Digital DLL

The NAND Flash DLL PHY IP contains logic that, in conjunction with I/O cell circuitry, addresses the timing requirements for data transfers between the ASIC and flash devices, which are asynchronous in nature. The delay compensation circuit was designed with the following features:

- Programmable read clock delay specified as a percentage of a clock cycle
- Programmable write data delays specified as percentages of a clock cycle
- Delay compensation circuit, re-sync circuitry activated during refresh cycles to compensate for temperature and voltage drift
- Separate delay chains for each read DQS signal from the flash devices

## Fully Portable Architecture

The soft PHY is structured in a netlist fashion, allowing cell logic to be easily inserted into the design. That allows the delay compensation circuit implementation to be easily migrated to different process technologies.

## NAND Flash Controller and Register Interfaces

The NAND Flash controller interface is compliant to DFI 3.0 with NAND optimizations. The register interface is a Cadence proprietary interface for configuration, calibration, and test modes.

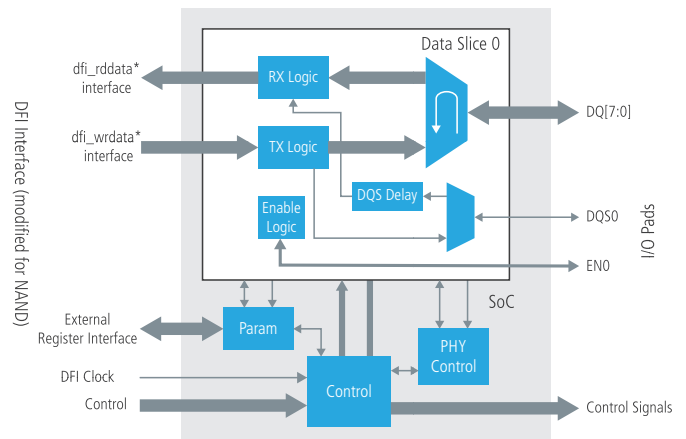


Figure 2: IP-Level Block Diagram

## DFT Implementation

The PHY supports Transition Fault testing of the digital logic at-speed, with a second pass at the lower frequency to target the faults in the configurable delay lines. Additional test mode has been introduced in the DLL PHY scan implementation for this purpose.

## Loopback Mode

The NAND Flash DLL PHY IP contains logic that allows for at-speed testing and data eye training without adding additional test multiplexers in critical timing paths in the design.

The loopback testing mechanism includes a vector generation unit, which creates patterns for the write data path and then tracks the data back through the read data path. Internal loopback testing can be used during production to verify that critical logic such as the DLL, write path, and read path are functioning correctly. External loopback can be used to test the at-speed connectivity of the I/O pads.

## Availability

The PHY IP is available with various configurations and supports the following protocols:

Protocols	Speed	Soft/Hard PHY
ONFI 4.1, 4, 3, 2, 1, Toggle 2,1, Async	600MHz	Soft

## Related Products

Part #	Description
IP6019	ONFI4.1 / Toggle 2 Controller IP
IP6016	ONFI4 / Toggle2 Controller IP
IP6017	ONFI2 Controller IP

## Deliverables

- Clean, readable, synthesizable Verilog RTL
- Synthesis and STA scripts
- Documentation including integration and user guide, release notes
- Verilog testbench with memory model, configuration files, and sample tests
- Verilog models of dummy I/O pads

For more information, visit [ip.cadence.com](http://ip.cadence.com)



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