cadence®

Design IP Brochure

Controller and PHY Automotive IP for Octal SPI Flash and HyperFlash

Overview

Flash memory storage is quickly expanding in Automotive, driven by Advanced Driver Assistance Systems (ADAS) and multimedia-rich Infotainment systems. Those applications require ever higher transfer rates and lower latency access to data. Expanding the flash Serial Peripheral Interface (SPI) bus from 4 I/Os (Quad SPI) to 8 I/Os (Octal SPI) doubles the Serial Flash throughput and provides a more efficient solution for emerging applications, while providing backwards compatibility with single, dual, quad, or octal I/O interfaces. HyperFlash uses HyperBus enabling shared bus with HyperRAM.

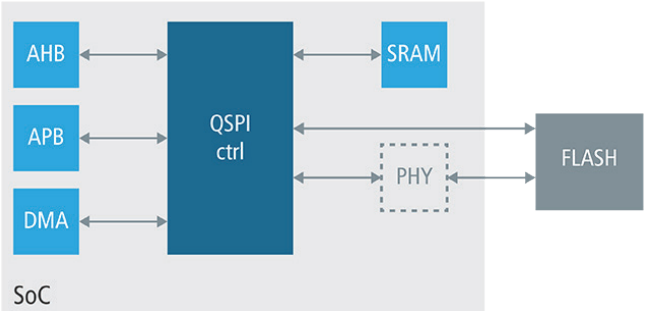

Figure 1: Example System-Level Block Diagram

Benefits

- Low-risk and silicon-proven design
- Customizable IP for easy integration with enhanced functional safety features
- Optimized for data transfer performance

The Cadence® Controller and PHY IP for Octal SPI Flash and HyperFlash supports 200MHz, with DDR Mode and Double Transfer Rate (DTR) Protocol enabling data transfer rates up to 400Mbps with reduced read latency, including support for Octal DDR protocol with DQS for Octal SPI devices. The improved performance enables Octal SPI designs to utilize continuous mode or eXecute In Place (XIP) with more efficiency and shorter access time, which accelerates overall system performance. The Controller IP was qualified using the strict Functional Safety requirements set by ISO 26262 standard.

The Controller IP connects to a system-on-chip (SoC) host through an ARM® AMBA® AHB bus, slave port, and APB bus for the register interface and optional DMA peripheral interface.

The integrated soft PHY enables the high clock rates, eliminating the reference clock at 4 times (4x) the bus when operating in SDR mode and 8x clock in DDR mode. That simplifies the SoC design, reduces the complexity of additional clock domains, and reduces power usage.

Key Features

- Enhanced active functional safety features
- Supports XIP (Execute in Place), DDR mode, single, dual or quad I/O instructions, BOOT and legacy modes
- Interoperable with Quad and Octal SPI devices from multiple vendors, including HyperFlash support
- Supports any device clock frequency, including current market device frequencies of 133MHz
- Programmable: device sizes, write protected regions, delays between transactions, interrupt generation
- Set of software APB accessible FLASH control registers to perform any FLASH command
- Programmable polarity, programmable baud rate generator, up to 4 external device selects
- Local SRAM to reduce AHB overhead and buffer FLASH data during indirect transfers

Product Details

The controller connects to SoC through its ARM AMBA AHB bus and APB bus interfaces. The AHB interface is used to transfer data, either in a memory mapped direct mode (e.g. execute code directly from Flash memory), or in an indirect mode (the controller is setup via configuration registers to silently perform some requested operation, signaling its completion via interrupts or status registers).

For indirect operations, data is transferred between system memory and external Flash memory via an internal SRAM, which is loaded for writes and unloaded for reads by an AHB master within the SoC at low latency AHB system speeds. Interrupts or status registers are used to identify the specific times at which this SRAM should be accessed using user programmable configuration registers. The size of the SRAM is configurable. An optional DMA peripheral bus is also available to optimize the data transfers between an external master and the controller during indirect transfers.

Developed by industry-leading domain experts, the Controller and PHY IP provides easy integration, reduced design risk, and faster time-to-market ASIC designs. Extensively validated using Cadence VIP and in use on multiple hardware platforms, the IP ensures first time right design saving the need for expensive time consuming re-spins.

Controller

The controller is waiting for valid access from AHB bus or for software trigger from the APB bus. When such an event occurs, the corresponding internal controller is selected (Direct Controller, Indirect Controller or Software-Triggered Instruction Generator). The block called Flash Command Generator arbitrates between accesses and forwards control into low-level SPI Module (low level SPI protocol controller).

PHY Module

The block above works on ref_clk. Data to transmit are synchronized from ahb_clk domain (clock of Flash Command Generator) to the ref_clk one in TX FIFO and then serialized to the external SPI Interface. When direction of transfer changes and device returns data to the controller, these are sent into RX FIFO and then synchronized from ref_clk domain to the ahb_clk one and then they are ready to be put on the AHB Bus.

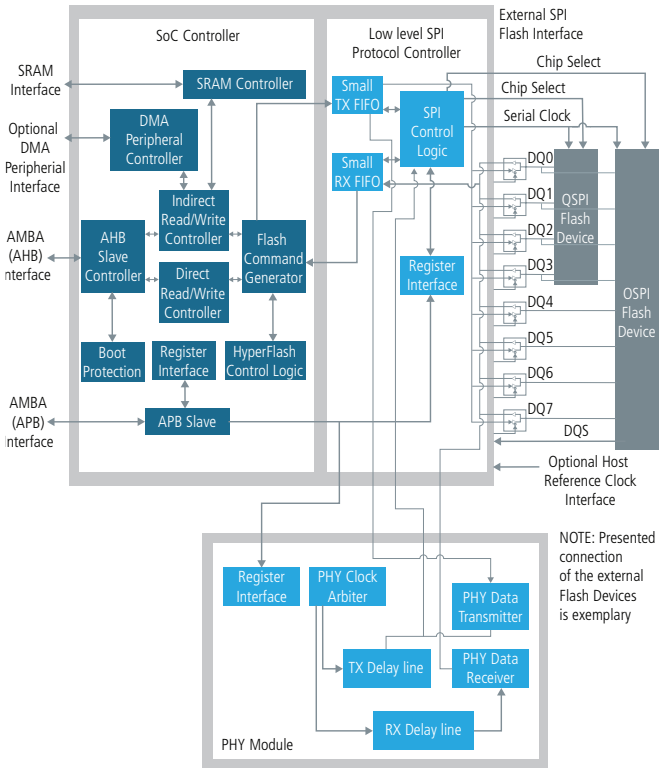

Figure 2: IP-Level Block Diagram

Functional Safety Features and Documentation

The controller and soft PHY include additional functional safety features targeting automotive applications. This includes memory protection using ECC, datapath and address parity protection, fatal fault detection, reporting and recovery mechanisms. The deliverables also include FMEDA report, safety manual and ISO 26262 ASIL readiness certificate.

Low Level SPI Protocol Controller

The SPI control logic selects source of datapath (with or without PHY) based on configuration. Note, ahb_clk and apb_clk are not directly used for low-level SPI transfer. Instead, the reference clock and its delayed variants are relevant for this type of transfer, with the PHY mode being enabled.

Availability

- Controller IP for Quad-Serial Peripheral Interface

Related Products

- Cadence VIP for Quad-Serial Peripheral Interface
- Cadence Controller and PHY IP for Octal SPI Flash
- Cadence Controller and PHY IP for Quad-Serial Peripheral Interface

Deliverables

- Clean, readable, synthesizable Verified HDL
- Cadence Encounter® RTL Compiler synthesis scripts
- Documentation—integration and user guide, release notes
- Sample verification testbench
- IP-XACT xml file

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