Ethernet Datasheet

Ethernet XAUI20 Physical Coding Sublayer (PCS) IP

Overview

Cadence IP Factory delivers custom, synthesizable IP to support specific design requirements.

The **Cadence Ethernet XAUI20 PCS IP** provides the logic required to integrate a XAUI20 PCS with a 10G Ethernet MAC (XGM) into any system on chip (SoC).

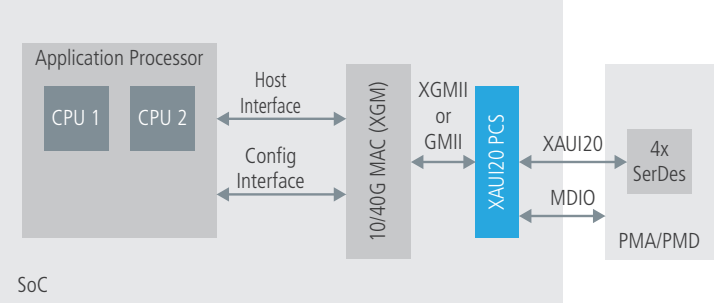

Figure 1: Example System Level Block Diagram

Compliant with IEEE Standard 802.3 and 802.3az, the **Cadence Ethernet XAUI20 PCS IP** has many configurable features and input parameters to customize the XAUI20 PCS for the specific needs of any application. The **Cadence Ethernet XAUI20 PCS IP** also supports Clause 36 of IEEE Standard 802.3 for applications requiring up to four Gigabit Ethernet ports.

The **Cadence Ethernet XAUI20 PCS IP** is architected to quickly and easily integrate into any SoC, and to connect seamlessly to a Cadence, or third-party, SerDes through a XAUI20 (4x20-bit) interface. Access from the MAC to the XAUI20 PCS is through a demultiplexed 64-bit XGMII interface, or a 4-port GMII interface.

Cadence IP Factory offers a comprehensive IP solution that is in volume production, and has been successfully implemented in more than 400 applications.

Key Features

- 64-bit demuxed XGMII works with Cadence XGM 10G Ethernet MAC
- Optional 1Gb/s mode with 4x GMII channels
- 20-bit data path reduces operating frequency
- Operates at 156.25MHz
- Built-in Idle conversion
- Lane synchronization and lane-to-lane alignment
- Optional MDIO interface for PHY management
- Support for IEEE 802.3az Energy-Efficient Ethernet
- 8b/10b encoding/decoding for each lane
- TX buffer option for phase compensation

Product Details

The **Cadence Ethernet XAUI20 PCS IP** provides the functionality of a physical coding sublayer (PCS) to facilitate full-duplex 10G, or optional 4x1G, Ethernet communication with a compliant MAC and XAUI-based SerDes.

Receive Path

For each lane, the receive path realigns unaligned data from the SerDes to the correct 10b boundary (comma alignment) before passing data to the 10b/8b decoder.

In the case of 10G operation, decoded data is sent to the CTC FIFO for over/underrun detection. Data from the four receive lanes is then passed to additional logic for lane-to-lane deskewing and idle replacement (realignment) prior to transmission to the MAC.

In the case of 1G operation, each lane operates as an independent 1G channel and does not require deskewing. Therefore, decoded data is sent directly from the 10b/8b decoder to an 8b-to-GMII converter for transmission to the MAC.

Transmit Path

For each lane, in the case of 10G operation the transmit path performs idle conversion and code group generation before passing data to the 8b/10b encoder. The 8b/10b encoder then sends encoded data to the SerDes.

In the case of 1G operation, each lane operates as an independent 1G channel and does not require idle conversion. Therefore, GMII traffic is sent to a GMII-to-8b converter for code group conversion before passing data to the 8b/10b encoder. The 8b/10b encoder then sends encoded data to the SerDes.

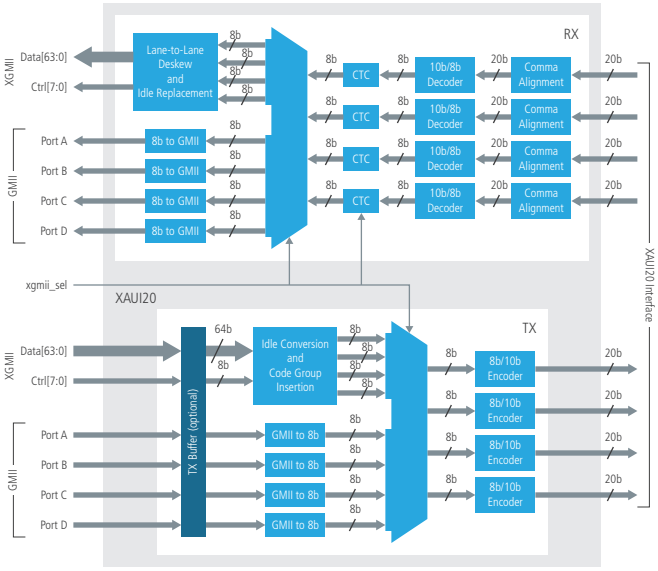

Figure 2: IP Level Block Diagram

An optional transmit buffer is available to decouple the XAUI20 PCS from the MAC for simpler clock tree insertion.

Cadence IP Factory

Cadence IP Factory can deliver various configurations of Ethernet PCS to meet your design requirements.

For more information, visit www.cadence.com/ip

Benefits

- Low Risk solutions – Silicon proven design
- Ease of Use – Customizable with easy integration
- Designed by an industry leader – Cadence is an active contributor to 802.3 standards working groups

Related Products

- Cadence® Verification IP for Ethernet
- 10/40G Ethernet MAC (XGM) IP
- 10GBASE-R Ethernet PCS (PCSR) IP
- 10/40G Ethernet PHY IP

Deliverables

- Verilog HDL
- Cadence® Encounter® RTL Compiler synthesis scripts
- User guide with full programming interface, parameterization instructions, and synthesis instructions
- Verilog testbench

Available Products

- Ethernet XAUI20 PCS IP
- Ethernet XAUI PCS IP

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