Design IP Brochure

PHY IP for USB 3.0/2.0 for TSMC

Overview

For over two decades, the Universal Serial Bus interface has truly lived up to its name - it has become the versatile connection standard that is present in a majority of electronic devices - laptops, mobile phones, portable electronics. After years of industry ubiquity of USB 2.0, USB 3.0 applications are becoming the preferred option due to close to 10x better performance to handle the growth of data that is being transferred between devices. And some devices need both for flexibly extend their market reach.

The Cadence® PHY IP for USB 3.0/2.0 is designed for this purpose, and operates in SuperSpeed (5Gbps), High-Speed, (480Mbps), Full-Speed (12Mbps), and Low-Speed (1.5Mbps) modes. The USB 3.0 PHY interface complies with PHY Interface for the PCI Express® and USB 3.0 Architectures, while the USB 2.0 PHY interface complies with the UTMI v1.05 specification.

The PHY IP is architected to quickly and easily integrate into any system-on-chip (SoC), and to connect seamlessly to a Cadence, or third party, PIPE-compliant and UTMI-compliant controllers.

The PHY IP provides a cost-effective, low-power solution for demanding applications. It offers SoC integrators the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs.

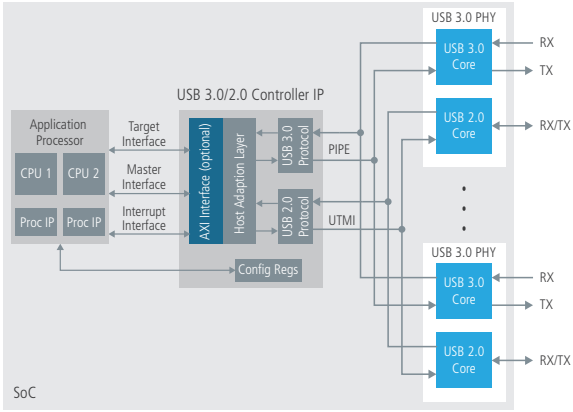

Figure 1: Example System-Level Block Diagram

Benefits

- **Ease-of-use—system integration kit reduces system integration and signal integrity issues**
- **Reduced test cost in mass production—BIST circuit**
- **Greater functional testing—datapath loopback**

The PHY IP is part of the comprehensive Cadence Design IP portfolio comprised of interface, Denali memory interface, analog, and systems and peripherals IP.

Key Features

- Integrated BIST pattern generator and checker with numerous programmable modes for stand-alone tests
- Low-power and ultra-low-power support through U0, U1, U2, and U3 power modes
- Programmable pre-emphasis and amplitude for the transmitter
- 8b/10b encoding/decoding implemented in hardware
- USB 2.0 PHY included for backward compatibility, as defined in USB specifications
- Support for full-swing and low-power swing transmitter

Product Details

The PHY IP is a hard PHY macro for the TSMC 28HPM/HPC processes. Integrated I/O pads and ESD structures are available.

The PHY IP supports the USB 3.0 and USB 2.0 specifications at speeds up to 5Gbps. It is designed to easily integrate with a Cadence USB controller, or any third party controller with PIPE-compliant and UTMI-compliant interfaces.

USB 3.0 Path

The USB 3.0 path of the PHY IP has separate transmit and receive channels for true full-duplex operation at SuperSpeed data rates (up to 5Gbps). The USB 3.0 path connects to a USB controller through a configurable PIPE interface to maximize throughput at different system bus clock frequencies.

USB 2.0 Path

The USB 2.0 path of the PHY IP is a mixed analog-digital design with High-Speed and Full-Speed/Low-Speed analog front ends, as well as with digital receivers and transmitters. The USB 2.0 path includes support for suspend mode to minimize power consumption when the IP is not in use. The USB 2.0 path connects to a USB controller through a 16-bit unidirectional UTMI interface.

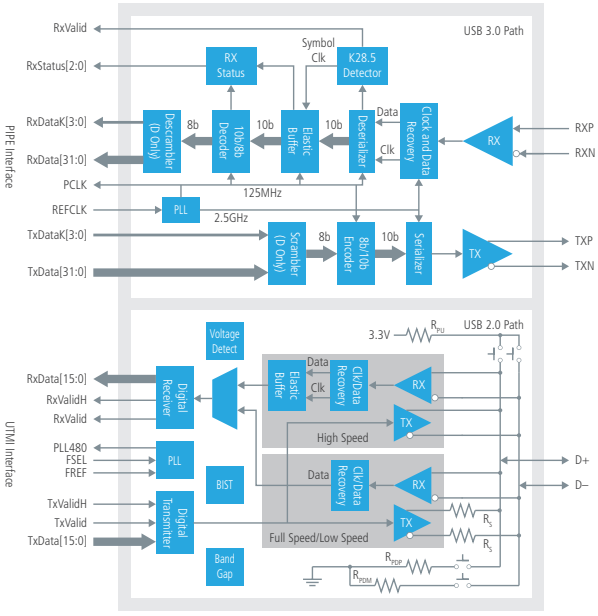

Figure 2: IP-Level Block Diagram

Availability

- Cadence PHY IP for USB 3.0/2.0 for TSMC 28HPM
- Cadence PHY IP for USB 3.0/2.0 for TSMC 28HPC

Related Products

- Cadence PHY IP for USB 2.0
- Cadence PHY IP for USB 3.0
- Cadence Controller IP for USB 3.0

Deliverables

- Verilog models for PHY modules
- Verilog testbench with configuration files and sample tests
- Clean, readable, synthesizable Verilog RTL with synthesis/STA scripts
- Liberty timing model
- SDF back-annotated timing verification
- Layout abstract in LEF format
- GDSII with at netlist for LVS
- LVS/DRC log files
- Documentation – specification sheet and integration/user guide

For more information, visit ip.cadence.com

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