Design IP Brochure

Denali Low-Power DDR PHY IP

Overview

The Cadence® Denali® Low-Power DDR PHY IP is an all-digital PHY IP consisting of a memory controller interface, external register interface (configuration and test), PHY control block (initialization and calibration logic), and any number of 8-bit data slices.

The PHY IP supports operation at twice the frequency of the memory controller and supports key low-power DDR SDRAM standards, LPDDR3, LPDDR2, DDR3, DDR3L, DDR2, at speeds up to 2400Mbps. It is architected to quickly and easily integrate into any system-on-chip (SoC), and to connect seamlessly to a Cadence, or third-party, DFI-compliant memory controller. Implemented on several popular processes. The IP provides a cost-effective, low-power solution for demanding applications. It offers SoC integrators the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs and implementations.

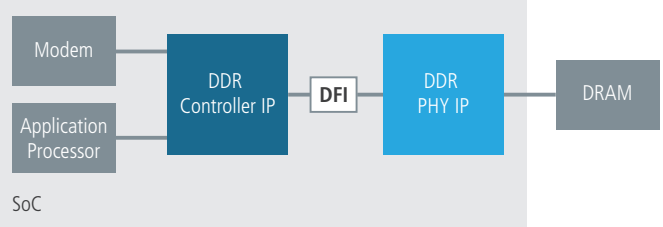

Figure 1: Example System-Level Block Diagram

Benefits

- **Widest possible data-valid-eye—DQS delay lines**
- **Expanded functional testing—datapath loopback**
- **Low-power control—clock gating**

The PHY IP a part of DDR product family, that can provide up to 3200Mbps. It's a perfect solution for low power and small area designs, that doesn't require latest speeds.

The PHY IP is part of the comprehensive Cadence Design IP portfolio comprised of interface, Denali memory interface, analog, and systems and peripherals IP.

Key Features

- Support for LPDDR3, LPDDR2, DDR2, DDR3, and DDR3L at speeds up to 2400Mbps
- LPDDR3/LPDDR2/DDR3 training including write-leveling and data-eye training through MC or PHY-Evaluation mode
- Optional clock gating available for low-power control
- Programmable clock delay (PVT compensated) on read and write datapaths for DQS alignment
- Memory Controller Interface complies with DFI 3.1, 3.0, 2.1, 2.0, and 1.0
- I/O pads with impedance calibration logic and data retention capability
- Register Interface for PHY programming, configuration, and testing modes
- Single PLL for low power and small area
- Boundary scan multiplexing built into core logic
- Per-byte deskew on read and write datapath

Product Details

The PHY IP is a classic DQS-delay architecture that uses programmable clock delay lines to align write data, read data capture, and DQS gating from the I/O pads across the DFI interface to the memory controller.

PHY Architecture

For total control over the DDR interface implementation, the PHY IP provides complete flexibility with process, library, floorplan, I/O pitch, packaging, metal stack up, routing, and other physical parameters.

The PHY IP is implemented with a slice-based architecture, which supports a wide range of memory classes and data rates. The data slice and CA slice provide flexibility for different protocols and data bus widths.

Data Slice and CA Slice

The data slice is an 8-bit wide design that interfaces to the DQ, DM, and DQS connections of the DRAM. The data slice is duplicated as many times as necessary to create the appropriate data width, allowing flexibility to adjust the data width to meet the requirements of the systems or applications. Depending on the configuration, a CA slice is provided for interfaces to the control, command, and address connections of the DRAM. The CA slice is duplicated as many times as necessary to create the appropriate width for different protocols or combination of protocols, allowing flexibility to adjust the number of control, command, and address signals as needed.

Memory Controller Interface

The memory controller interface is DFI 3.1, 3.0, 2.1, 2.0, and 1.0 compliant.

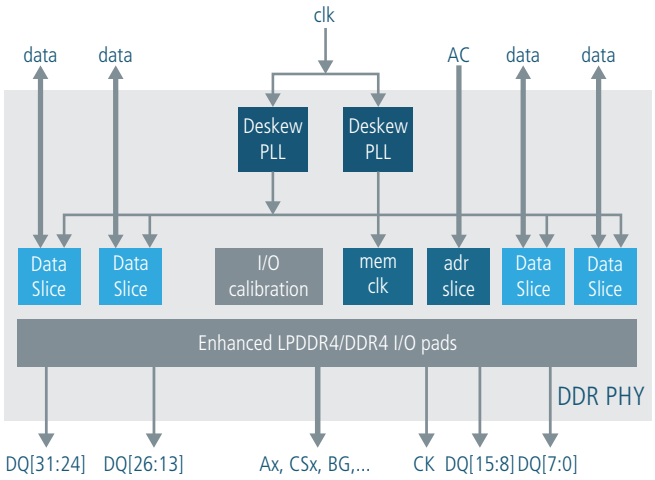

Figure 2: IP-Level Block Diagram

External Register Interface

The external register interface is a Cadence-proprietary interface to access the data slice registers.

PHY Control Block

The PHY IP control block provides initialization and calibration logic for training the DQS alignment for each data slice.

Availability

The PHY IP is available with various configurations and supports the following protocols:

Protocol	Speed	Process node
LPDDR3/2 DDR 3/3L/2	LP-2400	GF 28HPP
LPDDR3/2 DDR 3/3L/2	LP-1600	GF 28SLP
LPDDR3/2 DDR 3/3L/2	LP-1600	SMIC 28HK

Related Products

- Cadence Denali Controller IP for LPDDR 4/3/2
- Cadence Denali Controller IP for DDR 4/3/2
- Cadence Verification IP for Memory Models

Deliverables

- GDS II macros with abstract in LEF
- Verilog post-layout netlist
- STA scripts for use at chip or standalone PHY levels
- Liberty Timing model
- SDF for back-annotated timing verification
- Verilog models of I/O pads, and RTL for all PHY modules
- Verilog testbench with memory model, configuration files, and sample tests
- Documentation—integration and user guide, release notes
- Verification IP set up files

For more information, visit ip.cadence.com

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