

Advanced Programmable Interrupt Controller IP

Overview

Advanced Programmable Interrupt Controller provide optimized interrupt management. It is intended to solve interrupt routing efficiency issues in today's multiprocessor computer system applications.

The Cadence® Controller IP for Advanced Programmable Interrupt (APIC) is compliant with the ARM® AMBA® 2 specification and is designed to optimize interrupt handling performance by reducing latency, and providing prioritized nesting of interrupts.

Supporting up to 32 interrupt sources, including a single Fast IRQ-style interrupt, the Controller IP provides a cost-effective solution for demanding computer system applications. It offers system-on-chip (SoC) integrators the advanced capabilities and support that not only meet, but exceed the requirements of high-performance designs and implementations.

The Controller IP is architected to quickly and easily integrate into any SoC that supports an ARM AMBA 2 Advanced Peripheral Bus (APB).

This design IP is silicon-proven, with a over a 10-year history of reliable design-ins, and has been extensively validated with multiple hardware platforms.

The Controller IP is part of the comprehensive Cadence Design IP portfolio comprised of interface, memory, analog, and system, and peripheral IP.

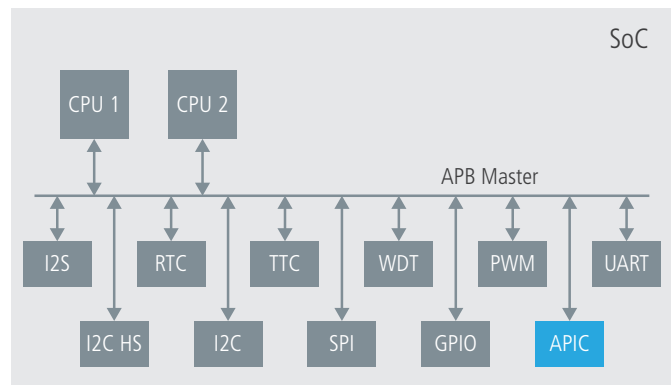


Figure 1: Example System-Level Block Diagram

Benefits

- **Low-risk solution—silicon-proven design**
- **Fully configurable—programmable source type, masking**
- **Easy integration—supports industry-standard APB interface**

Key Features

- Programmable edge triggered (rising, falling) or sensitive (high, low) trigger source
- Configurable number of interrupt sources (up to 31 IRQ, one fast IRQ)
- Selectable source for fast IRQ
- Supports up to 31 pending interrupt while servicing a single interrupt
- Eight levels of hardware priority
- Selectable hardware or software interrupt source
- Compliant with ARM AMBA 2 Specification
- All interrupt sources are maskable

Product Details

The Controller IP generates coded interrupt requests from up to 32 software and hardware interrupt sources. The number of interrupt sources can be set at compile time to help reduce gate count.

Priority Engine

The Controller IP is fully programmable, allowing software to individually enable and disable interrupt sources, and assign the Fast IRQ handler to any interrupt source. The priority of each interrupt source can be set to one of eight priority levels.

Trigger type can be programmed for each interrupt source individually. The Controller IP supports edge triggered (rising, falling) and level sensitive (high, low) interrupts. The interrupt source does not need to maintain the input level while the interrupt is being serviced.

APIC Registers

The Controller IP contains a full set of configuration registers for defining the APIC IP operation. Individual interrupt sources can be masked, preventing the source from generating an interrupt request while maintaining the priority level, trigger type (edge high-to-low, edge low-to-high, level high, level low) and status.

All registers are accessed through the APB interface.

IRQ and Fast IRQ Handlers

The IRQ handler generates an interrupt request once a valid interrupt is detected. Both a high level (irq) and low level (nirq) signal are generated, simplifying system design. Software can get information about the interrupt, and clear the interrupt, through the APB Interface.

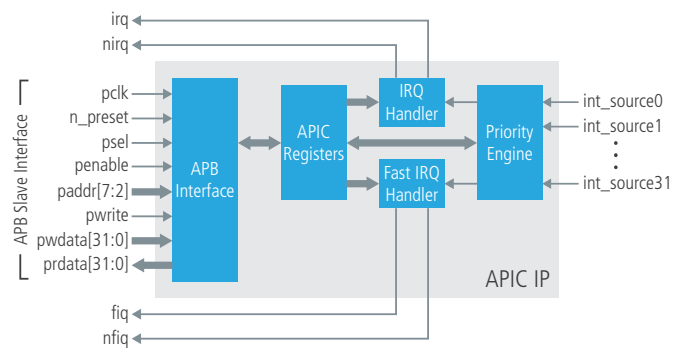


Figure 2: IP-Level Block Diagram

The Fast IRQ handler has separate high level (irq) and low level (nirq) interrupt requests similar to the IRQ handler. However, since the Fast IRQ handler is assigned to exactly one interrupt source, software does not need to read the APIC registers to determine the interrupt source. In addition, since the Fast IRQ handler has its own set of request signals, it does not need to use the priority logic to generate a request. Thus, the Fast IRQ service routine offers a considerable speed advantage over the IRQ service routine.

APB Interface

Target applications access the Controller IP through an APB slave interface.

Related Products

- Cadence Controller IP for Inter Integrated Circuit (I2C)
- Cadence Design IP for I2S Single Channel (I2S-SC) Bus Controller
- Cadence Design IP for I2S Multi Channel (I2S-MC) Bus Controller
- Cadence Controller IP for General Purpose Input Output (GPIO)
- Cadence Design IP for APB Serial Peripheral Interface (SPI) 32-bit
- Cadence Design IP for Universal Asynchronous Receiver Transmitter (UART)

Deliverables

- Clean, readable, synthesizable Verilog HDL
- Cadence Encounter® RTL compiler synthesis scripts
- Documentation—integration and users guide, release notes
- Sample verification testbench

For more information, visit ip.cadence.com

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