Overview

Today’s leading-edge mobile devices contain increasingly integrated functionality that enables growing volumes of content and video, more ways to control and interact, and longer battery life. The MIPI® Alliance defines semiconductor standards that support growing complexity and reduce device form factor. The Cadence® family of interface IP for MIPI protocols is leading the way with mobile-optimized low power and high performance. Compliant with the MIPI Specification for M-PHY with speeds up to 2.9Gbps per lane, the Cadence Design IP for MIPI M-PHY® also supports CSI-3™, LLI, and SSIC IP.

Developed by experienced teams with industry-leading domain expertise and extensively validated by multiple hardware platforms, the M-PHY IP is silicon-proven and shipping in high volume in multiple mobile devices. It is engineered to quickly and easily integrate into any design, and to connect seamlessly to a Cadence, or third-party, Reference M-PHY MODULE Interface (RMMI) compliant controller.

Implemented on several popular semiconductor processes, the M-PHY IP provides a cost-effective, low-power solution for demanding mobile applications.

The M-PHY IP is a mixed-signal PHY consisting of an M-PHY transmitter and an M-PHY receiver. It is developed and validated to reduce risk for designers so that their system on chip (SoC) can be first-time right. Developed and available early in the lifecycle of the most advanced semiconductor process nodes, it is designed to be robust under varying signal strength and noise conditions.

The M-PHY IP is part of the comprehensive Cadence Design IP portfolio comprised of interface, memory, analog, and systems and peripherals IP.

Key Features

- Compliant to MIPI Specification for M-PHY v2.0
- Mobile-optimized area and power
- Integrated BIST capable of producing and checking PRBS, CRPAT, and CJTPAT
- Matched analog design for low LANE-to-LANE skew and maximum timing margins
- Scalable up to four LANEs per SUB-LINK
- Receiver supports terminated/unterminated operation
- Configurable as Type-I or Type-II MODULE
- Slew-rate control for reduced EMI

Benefits

- Proven design in volume production
- Scalable LANE module with all low-power modes
- Evaluation platform enables faster time to market
**Product Details**

The M-PHY IP is a mixed-signal design that uses optimized and matched analog design for reducing LANE-to-LANE skew and maximizing timing margins. The full support of HS Gears with both Rate A and B, and Low-Speed signaling (LS-mode) provides great flexibility to further scale bandwidth to application needs.

**PHY Architecture**

The M-PHY IP employs modular implementation with scalability for up to four lanes in one sub-link. It provides excellent control over floor planning, placement and I/O integration while maintaining reliability and ease-of-use of the IP macro.

**Controller Interface**

The controller interface implements the RMMI found in Annex A of the specification for M-PHY. RMMI supports controllers based on MIPI CSI-3, UniPro, and LLI, and SuperSpeed USB Inter-Chip (SSIC) specifications.

**Transmitter and Receiver (M-TX and M-RX)**

When configured as a Type-I module, the M-PHY IP supports both high-speed (HS-MODE) and low-speed (LS-MODE) signaling. Transfer speeds up to 2.9Gbps per lane (HS-G2) are supported. PWM-BURSTs for low-power, low-speed operation (PWM-G1 to PWM-G5) are also supported.

**Availability**

The M-PHY IP is available with support for the following process node:

<table>
<thead>
<tr>
<th>Speed</th>
<th>Process node</th>
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<tbody>
<tr>
<td>2.9 M-PHY Gear 2</td>
<td>SMIC 28HK</td>
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**Related Products**

- Controller IP for SoundWire® Master, SoundWire Slave, CSI-2 Receiver, CSI-2 Transmitter, DSI Transmitter, SLIMbus® Device, SLIMbus Manager

**Deliverables**

- GDS II macros with abstract in LEF
- Verilog post-layout netlist
- STA scripts for use at chip or standalone PHY levels
- Liberty timing model
- SDF for back-annotated timing verification
- Verilog models of I/O pads and RTL for all PHY modules
- Verilog testbench with memory model, configuration files, and sample tests
- Complete technical documentation set
- Verification IP set up files

For more information, visit [ip.cadence.com](http://ip.cadence.com)

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