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Design IP Brochure

Controller and PHY IP for Quad Serial-Peripheral Interface

Overview

Flash memory is demanding ever higher transfer rates and lower latency. It is utilized frequently in computers and electronic devices found in automotive, IoT, drones, connected home, and other emerging applications. Expanding the flash Serial Peripheral Interface (SPI) accesses from the current 4 I/Os (Quad SPI) to 8 I/Os (Octal SPI) increases the Serial NOR Flash throughput and provides a more efficient solution for emerging applications, while providing backwards compatibility with support for single, dual, quad, or octal I/O interfaces.

The Cadence® Controller and PHY IP for Quad Serial-Peripheral Interface (QSPI) can be used to provide access to Serial Flash devices. Standard Serial Peripheral Interface (SPI) is supported along with high performance Dual and Quad SPI variants.

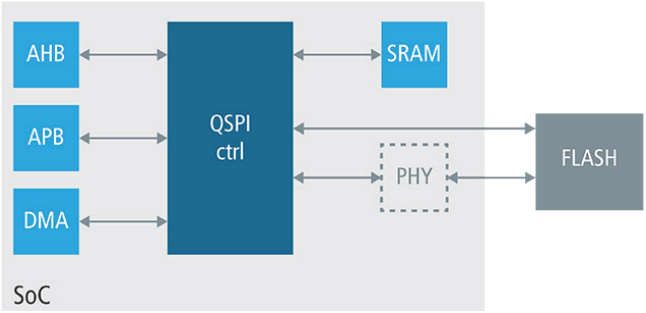

Figure 1: Example System-Level Block Diagram

Benefits

- Low-risk solutions—silicon-proven design
- Ease-of-use—customizable with easy integration
- Efficiency—optimized data transfer ensured

The Controller and PHY IP connects to system-on-chip (SoC) environment through its AMBA® AHB® bus and APB bus interfaces. The AHB interface is used to transfer data, either in a memory mapped direct fashion (for example a processor wishing to execute code directly from external Flash memory), or in an indirect fashion where the controller is setup via configuration registers to silently perform some requested operation, signaling its completion via interrupts or status registers.

For indirect operations of the Controller and PHY IP, data is transferred between system memory and external Flash memory via an internal SRAM which is loaded for writes and unloaded for reads by an AHB master within the system-on-chip (SoC) environment at low latency AHB system speeds.

An optional DMA peripheral bus is also available to optimize the data transfers between an external master and the Controller and PHY IP during indirect transfers.

Key Features

- Local SRAM of configurable size to reduce AHB overhead and buffer Flash data during indirect transfers
- Support for XIP (Execute in Place), DDR mode, single, dual or quad I/O instructions, BOOT and legacy modes
- Optional DMA peripheral interface to communicate indirect mode status with external DMA
- Supports any device clock frequency, including current market device frequencies of 133MHz
- Programmable: device sizes, write protected regions, delays between transactions, interrupt generation
- Set of software APB accessible FLASH control registers to perform any Flash command
- Serial clock with programmable polarity, programmable baud rate generator, up to four external device selects
- Compliant with AMBA2 specification

Product Details

The Controller and PHY IP is a controller that enables access to Serial Flash devices, while providing various modes of operation and improved high speed read data capture mechanism.

APB Interface and Register Module

The APB interface is used to configure the core and perform software controlled Flash accesses using the Flash Command Control register. The APB interface feeds a single register block containing the programmable register set. The register block is timed to the APB clock. All control or enable bits that are triggered by APB writes and cause an event to trigger, or an operation somewhere in the QSPI controller to be enabled are synchronized to the destination clock. Static configuration bits that have no effect while a separate enable bit is low do not require synchronization.

AHB Control Interface

The AHB slave controller validates incoming AHB accesses, responds to invalid requests, performs any required byte and half-word reordering, blocks writes that violate the programmed write protection rules (only for direct access) and forwards the transfer request to either the direct access controller or the indirect access controller.

Direct Access Controller (DAC)

Direct access refers to the operation where AHB accesses directly trigger a read or write to Flash memory. It is memory mapped and can be used to both access and directly execute code from external Flash memory. Any incoming AHB access that is not recognized as being within the programmable indirect trigger region is assumed to be a direct access and will be serviced by the direct access controller.

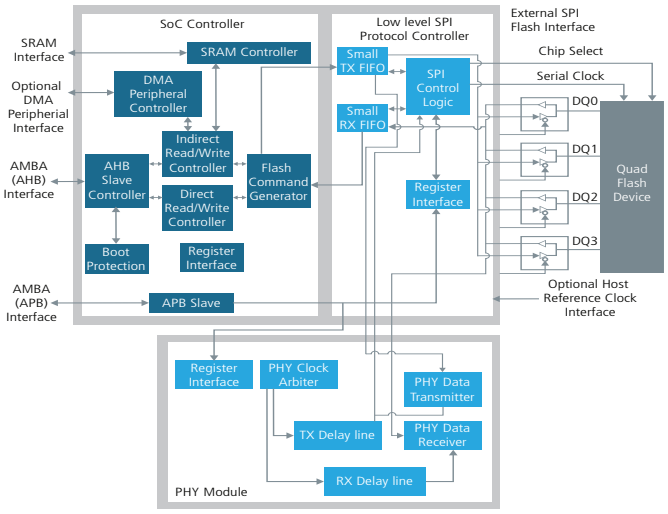

Figure 2: IP-Level Block Diagram

Indirect Controller (INDAC)

The aim of the indirect mode of operation is to read significant numbers of bytes from Flash memory without requiring an AHB access to trigger it. Instead indirect operations are controlled and triggered by software via specific APB control/configuration registers. This block will communicate with an embedded low level SPI protocol state machine module to perform an efficient and optimized Flash read burst, placing the read data into the local SRAM module ready for fast and low latency delivery to any external AHB master. Indirect transfer can be optionally performed along with external DMA Module. DMA Peripheral Controller ensures effective low-latency AHB transfers.

Availability

- Controller and PHY IP for Quad-Serial Peripheral Interface

Related Products

- Cadence Simulation VIP for SPI
- Cadence Controller and PHY IP for Octal SPI Flash
- Cadence Controller IP for Quad-Serial Peripheral Interface

Deliverables

- Clean, readable, synthesizable Verified HDL
- Cadence Encounter® RTL Compiler synthesis scripts
- Documentation—integration and user guide, release notes
- Sample verification testbench
- IP-XACT xml file

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