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Tensilica Datasheet

Tensilica ConnX BBE16 DSP for Baseband Processing

Configurable, extensible, scalable

The Cadence® Tensilica® ConnX BBE16 Baseband Engine is a high-performance digital signal processor (DSP) designed for use in LTE/4G modems and multi-standard broadcast receivers.

The ConnX BBE16 combines an 8-way single-instruction, multiple-data (SIMD), 3-issue very long instruction word (VLIW) 10-stage pipeline with a rich and extensible set of interfaces. Optimized for baseband complex number processing, the ConnX BBE16 provides a small footprint platform when compared against more generalized DSP platforms of its class.

The processing power of the ConnX BBE16 allows the system developer to go beyond the traditional approach of using a lightweight controller to exercise complex RTL blocks. A BBE16-based design can move many of the hardware functions into software running on the ConnX BBE16, increasing the flexibility of the design and reducing system complexity and development risk.

Features

- 16-way multiplier-accumulator (MAC), dual 8-way arithmetic logic unit (ALU) SIMD engines
- 3-issue VLIW for parallel load/store, MAC, and ALU operations
- 32-bit scalar ALU
- Supports a rich variety of complex arithmetic operations
- Single-cycle radix-4 fast Fourier transform (FFT) butterfly, 4 complex-tap finite impulse response (FIR), and 16 real-tap FIR operations
- Orthogonal frequency-division multiplexing (OFDM)- and multiple-input/multiple-output (MIMO)-optimized instruction set
- 160b-wide vector register file with support for:
  - 20b x 8
  - 40b x 4
- Dual 128b load/store units
- Optional instruction-set packages available:
  - 8-way SIMD integer and fractional divide
  - 4-way SIMD reciprocal square root
  - 16-way de-spread, including Hadamard Transforms
- Extensible interfaces with customized FIFO, port, and lookup interfaces
- High-performance C/C++ compiler with automatic vectorization of scalar C and full support for vector data

Benefits

- High performance, low power over a broad range of algorithms including support for LTE, HSPA+, and GPS
- Fast baseband development through familiar C programming with general-purpose DSP and 2G/3G/4G/Wi-Fi-specific library support
- Full support for hardware/software co-design
- Easy integration into system-on-chip (SoC) simulations with functional, cycle-accurate, and hardware pin-level models
- Extensible instruction set support through the Tensilica Instruction Extension (TIE) language
- Scalable with customized FIFO, port, and lookup interfaces

High Performance, Maximum Flexibility

Fast time to market, evolving standards, and long platform lives are all incompatible with the rigidity of ASIC-based designs. Only the deepest pockets can keep pace with changing standards based on fixed RTL designs.

Whether it's an Internet of Things (IoT) device, a data-only LTE modem, or a set-top box, all can benefit from the flexibility of a software-based solution. This flexibility can only be achieved by the use of modems that implement the signal processing on programmable processors.

From a LTE CAT 1 IoT modem to a CAT 4 2x2 MIMO modem, the ConnX BBE16 DSP offers the right blend of processing power and small footprint to build a low-power, low-cost SoC. The ConnX BBE16 DSP is built on Cadence's proven Tensilica Xtensa® LX customizable processor architecture and is specifically designed to support the needs of baseband signal processing. It delivers the processing capacity and flexibility needed for control-channel processing and other complex but infrequent operations such as cell search and paging channel monitoring. This allows you to minimize hardware accelerators in the processing chain, making the system not only more flexible, but also lower risk.

Beyond simple software programmability, support for push-button assembly of optimized processors is at the heart of all Xtensa processor-based ConnX products. This includes the ability to:

- Integrate targeted pre-built, verified function blocks
- Add/subtract from the basic instruction set
- Add full custom instructions through hardware (including full C programming support)
- Integrate the ConnX BBE16 core into complex systems through a variety of general-purpose and performance-optimized interfaces

Whether implemented as a single core, or a hybrid SoC made up of a ConnX BBE16 and hardware accelerator blocks, the ConnX BBE16 core is there to do the heavy lifting at the intersection of maximum performance and flexibility.

Configurable, Extensible, Scalable

The ConnX BBE16 Baseband Engine provides three pre-built vector options. These options are included/excluded as checkboxes when defining a core, and result in seamless integration of a feature into the hardware, the compiler, the modeling tools, and the verification scripts. In addition, the scalar unit within the ConnX BBE16 can be further extended through click-box options, including support for floating-point operations.

The ConnX BBE16 can be extended to support custom ports and queues for efficient connection to offload accelerators, which are fully supported in programming and modeling tools. These custom interfaces can be defined to match the interfaces of existing third-party intellectual property (IP). Thus, the ConnX BBE16 can access hardware offload accelerators in a single-cycle deterministic operation, greatly reducing power consumption and without impacting the shared system bus or the local memory subsystem.

Toolchain

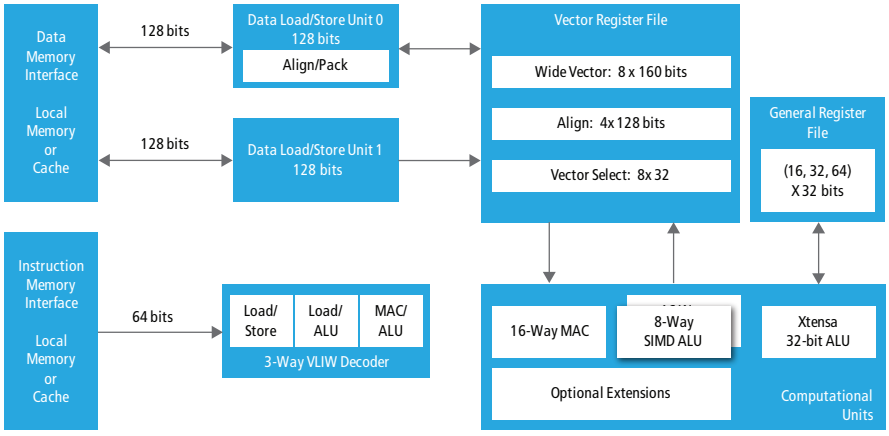
The ConnX BBE16 is delivered with a complete set of software tools. The toolset includes a high-performance C/C++ compiler with automatic vectorization to support the VLIW pipeline in the core. This comprehensive toolset also includes the linker, assembler, debugger, profiler, and graphical visualization.

Unlike many DSPs, a ConnX BBE16 programmer can work exclusively in C without the need to revert to assembly language. Comprehensive libraries provide access to highly optimized DSP functions, and more advanced libraries for functions (such as LTE modems) are optionally available. Access to specialized DSP instructions is available via C Intrinsics, and from there the tools take over, avoiding the need for the programmer to deal with the intricacies of register spills, instruction slotting, and scheduling conflicts. The result is productivity levels that are more consistent with general-purpose programming as opposed to the typical swamp associated with assembly language work.

A comprehensive instruction set simulator (ISS) allows you to quickly simulate and evaluate performance. When working with large systems or lengthy test vectors, the fast, functional TurboXim™ simulator option achieves speeds that are 40X to 80X faster than the ISS for efficient software development and functional verification.

Xtensa System C (XTSC) and C-based Xtensa Modeling Protocol (XTMP) system modeling can aid in full-chip simulations. Pin-level XTSC offers co-simulation of SystemC and RTL-level offload accelerator blocks for fast, cycle- accurate simulations.

The ConnX BBE16 supports all major back-end EDA flows, and represents the best in push-button customizable DSPs from Cadence, the leader in configurable, extensible, and scalable solutions for advanced communications systems. Its proven development environment for both hardware and software reduces time to market and risk, and provides maximum flexibility in baseband processing solutions for 4G, 3G, Wi-Fi, and beyond.



Simplified block diagram of a ConnX BBE16 Baseband Engine

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