cadence®

Design IP Brochure

10Gbps Multi-Protocol PHY IP

10G-KR, XFI, PCIe Gen 3/2/1, XAUI, QSGMII, SGMII, Gigabit Ethernet

Overview

Growing 10 Gigabit Ethernet deployments in the data centers and infotainment marketplace is driving the demand and connectivity needs of a broad range of high-end, energy efficient networking and computing applications.

Engineered for high-performance networking system and computing, the Cadence® 10Gbps Multi-Protocol PHY IP supports multiple interface standards, including 10GBASE-KR, XFI, PCI Express® (PCIe®) 3.0, XAUI, QSGMII, SGMII and 1G Ethernet for a flexible interconnect solution in System on Chip (SoC) designs.

The PHY IP is designed to deliver high eye-margin at low power for backplane application. Numerous auto-calibrated circuits, programmable state machines throughout the design for PHY performance tuning, and the LC tank PLL provide a low-power optimum performance design. PCIe low power states are also optimized to reduce total system power. All standard power states are supported.

The Cadence IP is engineered to quickly and easily integrate into any SoC, and to connect seamlessly with a Cadence, or third party, PIPE 4.0-compliant controller. The IP is silicon-proven in multiple process nodes and has been extensively validated with multiple hardware platforms.

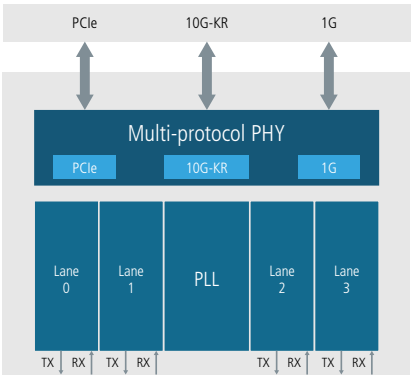

Figure 1: Example System-Level Block Diagram

Benefits

- Highly configurable for fastest SoC integration
- Long reach for demanding applications
- Graphical User Interface for eye monitoring

The Cadence 10Gbps Multi-Protocol PHY IP is part of the comprehensive Cadence Design IP portfolio comprised of interface, memory, analog, and system and peripheral IP.

Key Features

- Supports 10G-KR, PCIe Gen 3/2/1, XAUI, Q/SGMII, and GEthernet
- Automatic calibration of analog circuits and offset correction
- High performance Decision feedback equalization and adaptive CTLE
- LC tank PLL with a wide range of reference clock frequencies and SSC
- Available in X1 through X10 lane configurations
- Serial and parallel loop-back functions
- Bifurcation and inverse bifurcation support
- On-chip Eye & Bathtub Monitor
- High performance Decision feedback equalization and adaptive CTLE
- Configurable PMA/PCS parallel interface

Product Details

The Cadence 10Gbps Multi-Protocol PHY IP is a hard PHY macro available for TSMC processes. I/O pads and ESD structures are included. It is designed to easily integrate with a Cadence Controller IP for PCIe, or any third party controller with a PIPE 3.0- or PIPE 4.0-compliant interface.

Architecture

The Cadence 10Gbps Multi-Protocol PHY IP macro consists of a Physical Media Attachment (PMA) layer and a Physical Coding Sublayer (PCS). Optimized for 10G Ethernet and PCIe 3.0 applications, the PHY IP provides long reach performances at low power with low area.

Compliant with IEEE Standard 802.3 10GBASE-KR requirements (Clause 51) and PCIe 3.0, 2.0, and 1.1, the Cadence 10Gbps Multi-Protocol PHY IP is highly-configurable allowing the PHY to be customized to your specific needs.

The Cadence 10Gbps Multi-Protocol PHY IP is designed with a lane-based architecture featuring one common support for up to 10 lanes, providing greater control over floor planning, placement, packaging, and I/O integration than other hard PHY solutions, while maintaining reliability and ease of use associated with GDSII macros. On-chip PLL is compatible with selected reference frequency up to 156.25 MHz with an available PLL lock status pin.

The PCS portion of the PHY provides the control, encoding and protocol logic. The architecture partitions the PMA core into different primary sub-modules: common PLL, transmitter, and receiver lane modules. The PMA block provides the transmit, common PLL and receive functions. The common PLL module

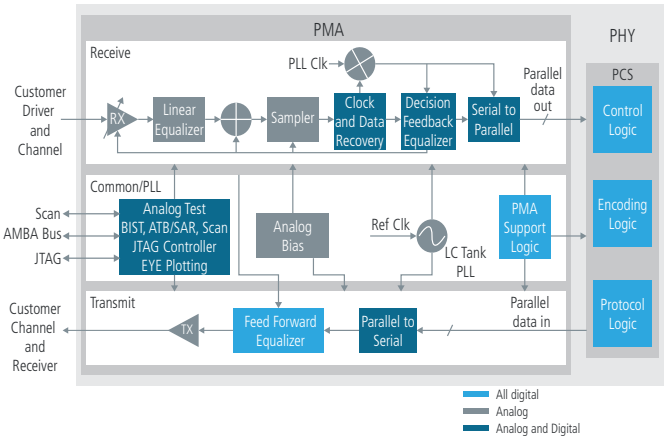

Figure 2: IP-Level Block Diagram

provides the interface between Scan, AMBA Bus and JTAG and Analog Test including BIST, ABT/SAR, Scan, JTAG control, EYE plotting and PMA support logic functions.

The transmitter module converts parallel data from the PCS interface to a serial data stream. The receiver module converts an input serial data stream to parallel data going to the PCS interface.

The Cadence 10Gbps Multi- Protocol PHY IP can be delivered in x1 to x16 configurations for PCIe, and 4x10G, 10x10G and 1G for Ethernet. As an active member of many standards organizations, Cadence has early insight into emerging standards, and can quickly and easily adapt to critical and important changes to current standards.

Availability

The 10Gbps Multi-Protocol PHY IP is available in FlipChip with various speeds, protocols and process nodes as follows:

Speed	Protocol	Process
10Gbps/8Gbps	10Gbps Multi-Protocol PHY (+PCIe3)	TSMC 28HPC+
10Gbps/8Gbps	10Gbps Multi-Protocol PHY (+PCIe3)	TSMC 28HPC
10Gbps/8Gbps	10Gbps Multi-Protocol PHY (+PCIe3)	TSMC 28HPM

Related Products

- Controller IP for PCIe 3.0
- 10/40G Ethernet MAC (XGM) IP

Deliverables

- Standard integration views such as: LEF abstract, timing views (.LIB), behavioral model (Verily), gate-level netlist, SDF, DRC, LVS, ANT reports and GDSII layout and layer map
- Synthesizable soft PCS with SDC
- Complete documentation including user guide, integration guide, and programmer guide
- High Volume Manufacturing (HVM) kit
- Testboards available upon request

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