cadence®

Design IP Brochure

Denali Controller IP for DDR

LPDDR 4/3, DDR 4/3/3L, up to 3200Mbps

Overview

Today's device users demand quick response time and high resolution images which require electronics systems to process higher volumes of data and video, exploding the required capacity and bandwidth for device memory. Cadence® solution is the Cadence Denali® DDR IP family of high-speed on-chip interface IP to external memories, with the bandwidth necessary to support these applications. The Cadence Denali Controller IP for LPDDR 4/3 and DDR 4/3/3L provides low latency and up to 3200Mbps throughput, while supporting extensive value added features including, but no limited to reliability features.

Developed by experienced teams with industry-leading domain expertise and validated with multiple hardware platforms, the Controller IP is silicon proven and can provide customers with ease of integration and faster time-to-market.

The Controller IP is engineered to quickly and easily integrate into any system-on-chip (SoC), and is verified with the Denali DDR PHY IP as part of a complete memory subsystem solution which also includes Cadence VIP. The Controller IP is designed to connect seamlessly and work with a third-party, DFI-compliant DDR PHY IP.

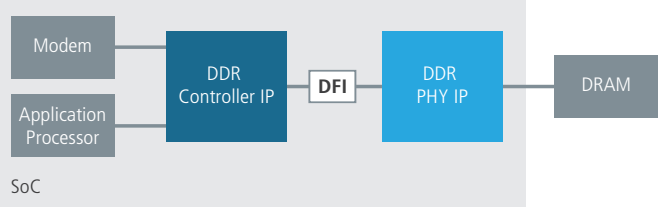

Figure 1: Example System-Level Block Diagram

Benefits

- **Configurable to meet specific data traffic profiles**
- **Optimized low latency for data-intensive applications**
- **Future-proof system design for emerging DDR standards**

The Controller IP is developed and validated to reduce risk for the customer, so that their system-on-chip (SoC) can be first time-right. Developed for and available in alignment with the PHY IP on advanced semiconductor process nodes, the Controller IP is designed to be robust under various traffic loads and to have interoperability with various supplier memory chips.

The Controller IP is part of the comprehensive Cadence Design IP portfolio comprised of Interface, Denali memory interface, analog, and systems and peripherals IP.

Key Features

- Compliant to LPDDR 4/3 and DDR 4/3/3L protocol memories
- DDR4/3 In-line ECC
- Single and multi-port host interface options
- Flexible paging policy including auto-precharge-per-command
- Supports advanced RAS features including SEC/DED ECC, error scrubbing, parity, etc.
- Priority-per command on ARM® AMBA®3 AXI and low latency Denali interface
- QoS features allow command prioritization on ARM AMBA4 AXI interfaces
- Silicon proven and shipping in volume

Product Details

The Controller IP is designed to provide the flexibility needed to enable application specific configurations ranging from high performance networking and mobile to consumer. The host side port interface can be configured to support multiple ports, each of varying width and with different AMBA protocol and clocking options. The command queue intelligently schedules traffic from the port arbiter to maximize data throughput efficiency. The Controller IP includes various feature options such as low power modes required by mobile applications and several reliability features required by enterprise applications.

DDR DRAM Controller

The Controller IP was engineered to be highly configurable allowing the selection of application specific features, which in turn yields an area optimized solution per application. The controller is also developed to provide maximum throughput across many different traffic profiles.

The Controller IP uses multi-stage reordering algorithms architected for use with traffic profiles from many different applications. Performance-tuning parameters allow performance optimization based on individual system and memory requirements.

The Controller IP includes optional features to support high density system requirements including RDIMM, LRDIMM as well as 3DS and x4 DRAM devices.

The Controller IP also delivers a wide array of capabilities to address emerging DDR DRAM subsystem RAS (Reliability, Availability and Serviceability) requirements. Some of these capabilities include embedded support for ECC and other vital error detection and error prevention capabilities such as parity protection and DRAM data scrubbing. All the Controller IP configurations support power-down and self-refresh. The optional advanced low power module includes automatic power level stepping (based on traffic). This level of low-power support can significantly reduce standby and active power. A security option for address range protection is also available.

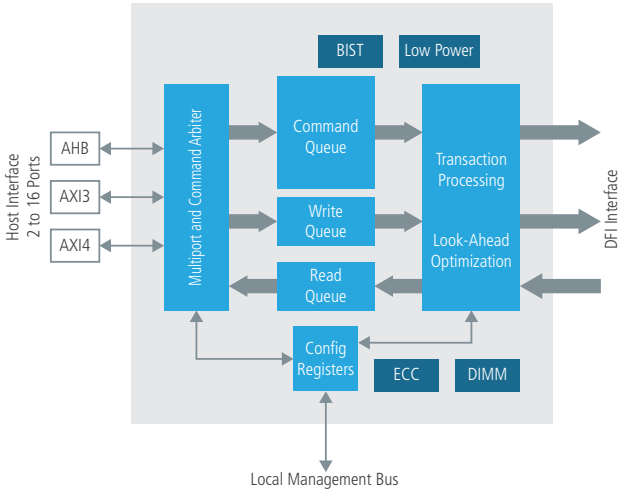

Figure 2: IP-Level Block Diagram

Host Interface

Natively supports any mix of AHB and AXI interfaces, up to 16 buses. Priority-per-command on AXI3 interfaces, and QoS on AXI4 interfaces improves latency and controller QoS, especially for transactions delivered through an interconnect fabric. Flexible synchronization allows low-latency synchronous port connection, reduced-latency pseudo-synchronous ratio port connection, or highly flexible asynchronous port connection.

DFI Interface

The DFI-compliant PHY interface connects to Cadence, or third-party, hard and soft PHYs.

Availability

The Controller IP is available with various configurations and supports the following protocols:

Protocol	Speed
LPDDR4/3	up to 3200Mbps
DDR4/3/3L	up to 3200Mbps

Related Products

- DDR Subsystem—integrated controller, PHY, and software
- LPDDR/DDR PHY IP
- DDR PHY IP

Deliverables

- Clean, readable, synthesize-able Verilog RTL
- Synthesis and STA scripts
- Documentation—integration and user guide, release notes
- Sample Verification testbench with integrated BFM and monitors

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