

# Simulation VIP for Display Stream Compression (DSC)

## Overview

Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.

## Specification Support

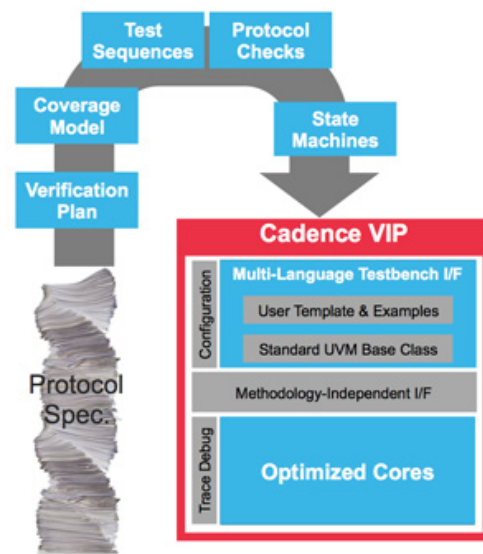
The Cadence DSC VIP Plugin supports DSC 1.2 for Embedded DisplayPort (eDP) versions 1.4b.

The Cadence DSC VIP Plugin supports DSC 1.1 for MIPI Display Serial Interface protocols family, DSI 1.3.1 and DSI-2 1.0.

The specifications are available here: <http://www.vesa.org>

## Supported Design-Under-Test Configurations

- Master
- Slave
- Full Stack



## Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification.

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## Key Features

### eDP 1.4b

- Configuration includes Discovery, Enabling, Disabling
  - Framing and Compressed Stream Mapping of 1, 2 or 4 slices per line
  - Picture Parameter Set (PPS) Packet value cannot be verified as there are no specified constraints in DSC
  - DPCD fields use status, control, and capability registers
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### MIPI DSI and DSI-2

- Video frames encoded using Display Stream Compression algorithm are decoded by VIP monitor
  - Active Processor VIP generates video frames encoded using Display Stream Compression algorithm
  - VIP verifies format correctness of DSI packets related to Display Stream Compression
  - VIP verifies content correctness of DSI packets related to Display Stream Compression
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## Related Products

- DisplayPort Simulation VIP
- DisplayPort 8K Simulation VIP
- MIPI Display Serial Interface Simulation VIP
- MIPI Display Serial Interface 2 Simulation VIP



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