VIP Datasheet

Simulation VIP for Time Sensitive Network (TSN)

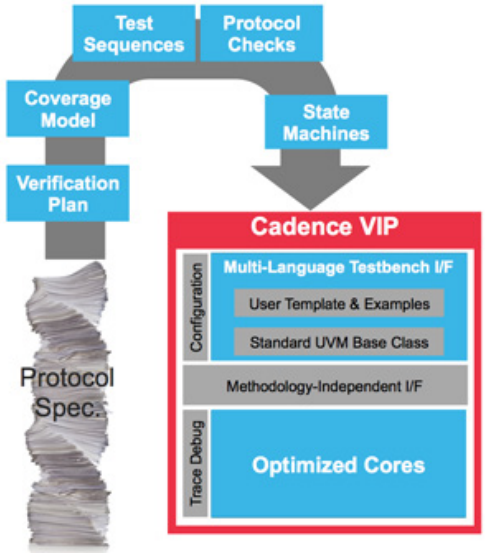
Supports Energy Efficient Ethernet (EEE)

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

Cadence TSN VIP is compliant with the 802.1 TSN Specifications created by the Time Sensitive Networks Task Group of IEEE. TSN specifications are developed and maintained by IEEE. They can also be obtained on request from IEEE or viewed at

http://www.ieee802.org/1/pages/tsn.html

Standards Supported

- IEEE 802.1AS
- IEEE 802.1Qbu
- IEEE standard 802.1AE
- IEEE 802.3br
- IEEE 802.3az
- IEEE 802.1Qav

Supported Design-Under-Test Configurations

☑ MAC	☐ PHY	☐ Hub/Switch
☑ Full Stack	☐ Controller-only	☐ PHY-only

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the "raw" coverage model results back to the protocol specification.

Key Features

- Precision Timing protocol provides synchronised timing information between different network nodes; selects best clock to be used for creating time domains
- PTP peer delay protocol used to measure propagation delay on the link
- Synchronization information transported using PTP messages Sync and Follow_Up.
- Best Master Clock Selection Algorithm determines grandmaster for a gPTP domain.
- Credit Based Shaping scheduling algorithm to ensure bandwidth utilisation by different classes of traffic is equitable
- Supports Preemption: Forwarding and queuing protocol to ensure long ethernet application frames do not hamper transfer of shorter high priority interrupt and command messages sent from sensors to ECUs.
- Interspersing provides capability to preempt lower priority Pre-emptable frame when high priority Express frame is forwarded by Preemption block.
- MACSec security feature provides authentication and encryption capability for Ethernet frames across links. Based on AES-128 and AES-256.
- Energy Efficient Ethernet

Related Products

- Ethernet Simulation VIP
- Ethernet Accelerated VIP

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