VIP Datasheet

Simulation VIP for DisplayPort 8K

Supports Display Stream Compression (DSC)

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

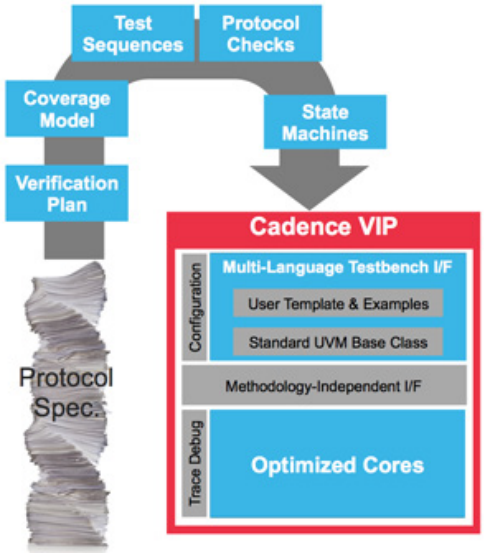
The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.

Specification Support

The Cadence DisplayPort 8K VIP provides support, for 8.1Gbps per lane protocols, DisplayPort 1.3 and 1.4, and Embedded DisplayPort (eDP) versions 1.4a and 1.4b. The specifications are available here: http://www.vesa.org

Supported Design-Under-Test Configurations

☑ Master ☑ Slave ☑ Full Stack



Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the "raw" coverage model results back to the protocol specification.

Key Features

DisplayPort 1.3

- Supports YCbCr 420 bpp 12, 15, 18, 24 and bpp 6,7,8,10,12, 14,16
- Supports Camera SDP and VSC SDP extentions for Pixel Encoding/Colorimetry format
- Includes Extend MSA Timing Parameters Ignore option
- Supports HBR3 (8.1 Gbps/lane speed), TPS4 and Post LT link training
- BT2020 and MISC 1 bit 6 support
- Supports addition of all link quality measurement test patterns
- Incorporates “End of active line TU clarification” SCR
- Enables Adaptive-Sync v3 SCR; ignore MSA

DisplayPort 1.4

- Supports Camera SDP, VSC SDP Extentions for VESA and CEA
- Supports CEA InfoFrame SDP packing format Ver.1.3
- Enables picture parameter set SDP (see more in DSC section)
- Enables multiple AUK_ACKs during link training
- Supports partial training patterns

eDP 1.4a and eDP 1.4b

- Supports Advanced Link Power Management (ALPM) to reduce wakeup latency and additional updates
- Modified requirements for Fast Wake Timing
- PSR updates: Added support for Y-coordinate; Enabled new selective update X and Y coordinate increment granularity limits and synchronization latency in Sink device

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