

Controller and PHY IP for Octal SPI Flash

Overview

Flash memory is used frequently in computers and electronic devices found in Automotive, IoT, Drones, Connected Home, and other emerging applications, and is demanding ever higher transfer rates and lower latency. Expanding the flash Serial Peripheral Interface (SPI) accesses from the current 4 I/Os (Quad SPI) to 8 I/Os (Octal SPI) increases the Serial NOR Flash throughput and provides a more efficient solution for emerging applications, while providing backwards compatibility with support for single, dual, quad, or octal I/O interfaces.

The Cadence® Controller and PHY IP for Octal SPI Flash supports the fastest access frequency of 200MHz, with DDR Mode and Double Transfer Rate (DTR) Protocol enabling data transfer rates up to 400Mbps with reduced read latency, including support for Octal DDR protocol with DQS for Octal SPI devices. The improved performance enables Octal SPI designs to utilize continuous mode or Execute in Place (XIP) with more efficiency and shorter access time, which accelerates overall system performance.

The Controller and PHY IP connects to a system-on-chip (SoC) host through an ARM® AMBA® AHB bus, slave port, and APB bus for the register interface and optional DMA peripheral interface.

The integrated soft PHY enables the highest speed clock rates, eliminating the reference clock at 4 times (4X) the bus when operating in SDR mode and an 8X clock in DDR mode. That simplifies the SoC design, reduces the complexity of additional clock domains, and reduces power used by the Octal SPI bus.

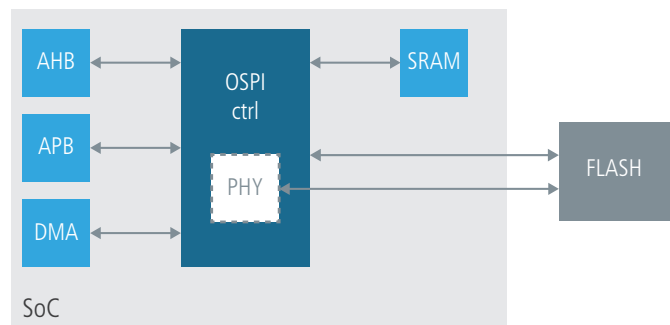


Figure 1: Example System-Level Block Diagram

Benefits

- **Flexibility**—several SPI protocols with single IP allows for single SoC design for several derivatives (low/mid/high-end)
- **Simplicity**—using soft PHY simplifies SoC timing design
- **High performance**—supports maximum Octal SPI data rates and XIP

Key Features

- Software triggered 'indirect' mode for low latency data transfers
- Independent reference clock to decouple AHB clock from SPI clock – allows for slow system clocks
- Up to 200MHz DDR (with DQS) for Octal SPI devices
- Memory mapped 'direct' mode for XIP
- Up to 133MHz SDR or 80MHz DDR for Quad SPI devices
- Support BOOT mode and XIP (eExecute In Place)

Product Details

The controller connects to the SoC through its ARM AMBA AHB bus and APB bus interfaces. The AHB interface is used to transfer data, either in a memory mapped direct mode (e.g. execute code directly from Flash memory), or in an indirect mode (the controller is setup via configuration registers to silently perform some requested operation, signaling its completion via interrupts or status registers).

For indirect operations, data is transferred between system memory and external Flash memory via an internal SRAM, which is loaded for writes and unloaded for reads by an AHB master within the SoC at low latency AHB system speeds. Interrupts or status registers are used to identify the specific times at which this SRAM should be accessed using user programmable configuration registers. The size of the SRAM is configurable. An optional DMA peripheral bus is also available to optimize the data transfers between an external master and the controller during indirect transfers.

Developed by industry-leading domain experts, the Controller and PHY IP provides easy integration, reduced design risk, and faster time-to-market ASIC designs. Extensively validated using Cadence VIP and in use on multiple hardware platforms, the IP ensures first time right design saving the need for expensive time consuming re-spins.

Controller

The controller is waiting for valid access from AHB bus or for software trigger from the APB bus. When such an event occurs, the corresponding internal controller is selected (Direct Controller, Indirect Controller or Software-Triggered Instruction Generator). The block called Flash Command Generator arbitrates between accesses and forwards control into low-level SPI Module (low level SPI protocol controller).

PHY Module

The block above works on ref_clk. Data to transmit are synchronized from ahb_clk domain (clock of Flash Command Generator) to the

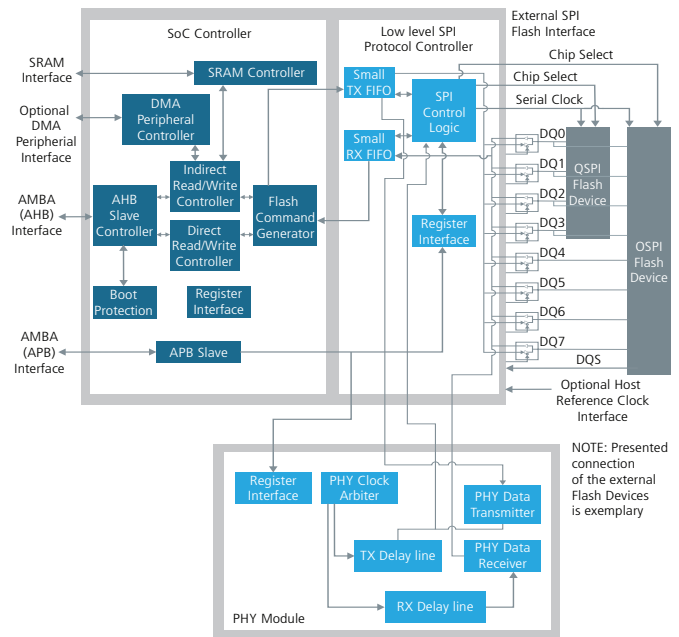


Figure 2: IP-Level Block Diagram

ref_clk one in TX FIFO and then serialized to the external SPI Interface. When direction of transfer changes and device returns data to the controller, these are sent into RX FIFO and then synchronized from ref_clk domain to the ahb_clkone and then they are ready to be put on the AHB Bus.

Low Level SPI Protocol Controller

The SPI control logic selects source of datapath (with or without PHY) based on configuration. Note, ahb_clk and apb_clk are not directly used for low-level SPI transfer. Instead, the reference clock and its delayed variants are relevant for this type of transfer, with the PHY mode being enabled.

Availability

The Controller and PHY IP is available with various configurations and supports the following protocols:

Protocol	Speed
Octal SPI	166MHz SDR (with DQS)
Octal SPI	200MHz DDR (with DQS)

Related Products

- Cadence Controller IP for Quad Serial-Peripheral Interface (QSPI)
- Cadence Controller and PHY IP for Quad Serial-Peripheral Interface (QSPI)

Deliverables

- Clean, readable, synthesizable Verilog HDL
- Cadence Encounter® RTL compiler synthesis scripts
- Verilog testbench with memory model, configuration files, and sample tests
- Documentation—integration and user guide, release notes

For more information, visit ip.cadence.com



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