Design IP Brochure

Gigabit Ethernet MAC IP

Overview

Industrial and Infrastructure system architects look to faster Ethernet speeds to solve increased bandwidth demands. With a comprehensive and rich feature set, multiple integration options and flexible configurations, Cadence is leading the way in mainstream Ethernet IP.

Compliant with IEEE Standard 802.3, the Cadence® IP for Gigabit Ethernet MAC is highly customizable with support for an integrated 1000BASE-X PCS, a high performance DMA with advanced AXI offloading features and descriptor caching, QoS, 1588 and TSN/AVB features to support any application. It supports a host of other features including IEEE 802.3az Energy-Efficient Ethernet (EEE), VLAN, TCP/IP offload and remote network monitoring (RMON).

The MAC IP is engineered to quickly and easily integrate into any SoC, and to connect seamlessly to a PHY through standard media independent interfaces such as MII, RMII, GMII, RGMII, SGMII and TBI. Host layer access to the GEM is through industry-standard AXI and AHB interfaces or through an external FIFO interface with or without DMA. A separate APB interface allows the host application to configure the GEM.

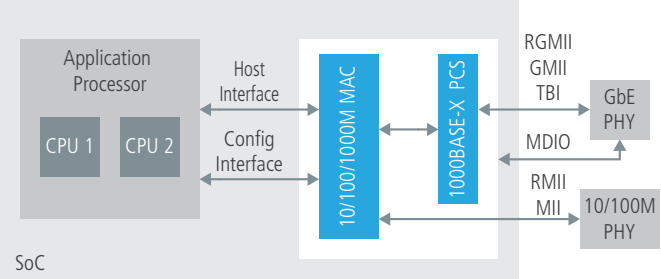

Figure 1: Example System-Level Block Diagram

Benefits

- Feature rich and compliant with the latest standards
- Flexible configuration with choice of integrated PCS interfaces and with a core driver to go with it
- Silicon proven and widely licensed

The MAC IP is silicon-proven and has been in production with multiple devices in the field. The MAC IP is part of the comprehensive Cadence Design IP portfolio comprised of interface, memory, analog, and system and peripheral IP.

Key Features

- IEEE 802.3 compliant, UNH tested
- Integrated 1000BASE-X PCS
- Support for MII, RMII, GMII, RGMII and TBI interfaces
- AXI4, AHB and DMA support
- TSN/AVB protocol support
- 802.3az Energy-Efficient Ethernet support
- 802.1Q and 802.1ad VLAN support
- Wake-on-LAN Support
- TCP/IP offloading capability
- Programmable jumbo frames up to 16,383 bytes

Product Details

The MAC IP supports integrated 1000BASE-X PCS, DMA, 1588 protocol, TSN/AVB protocols and 802.3az EEE.

Gigabit Ethernet MAC (GEM)

The MAC IP is compliant with IEEE 802.1Qbb priority-based flow control (PFC) with support for up to 16 priority queues and pause frames on both TX and RX. GEM supports virtual LANs by IEEE 802.1Q VLAN tagging with recognition of incoming VLAN and priority-tagged frames. It provides address checking logic for up to 32 specific Ethernet (MAC) addresses, four type IDs, hash matching of unicast and multi-cast destination addresses and wake-on-LAN. GEM is capable of offloading TCP/IP and UDP functions such as checksum, TCP Segmentation Offload (TSO), UDP Fragmentation Offload (UFO) and Receive Side Coalescing (RSC). GEM performs padding and CRC generation for transmit frames, and comes with statistics counters for RMON/MIB support.

Time Sensitive Networking (TSN) and Audio Video Bridging (AVB)

Time sensitive applications require timely and reliable data transfer with minimum latency addressed by TSN/AVB features supported by GEM. It supports time synchronization protocols such as IEEE 1588 and 802.1AS precision time protocol (PTP) via a Time Stamping Unit (TSU). For traffic management, features such as 802.1Qav (Credit Based Shaping), 802.1Qbv (time aware scheduling), 802.1Qbu/802.3br (frame pre-emption) and algorithms such as Fixed Priority, Deficit Weighted Round Robin (DWRR) and ETS (Enhanced Transmission Selection, or 802.1Qaz) are supported.

Dynamic Memory Access (DMA)

The DMA is an AXI4 or AHB master that improves performance and allows connections to system fabrics. It supports features such as support for up to 16 outstanding transactions that can cross frame boundaries to maximize pipelining of transfers, configurable

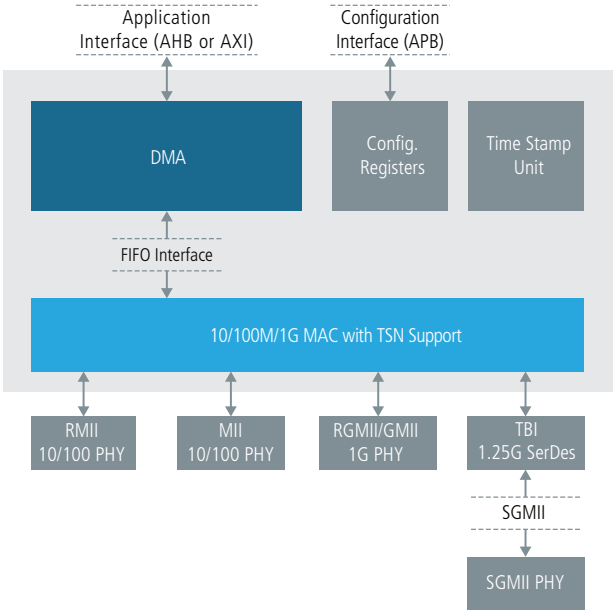

Figure 2: Example System-Level Block Diagram

descriptor buffers for further performance boost, programmable burst length and endianness options to maximize burst efficiency. The DMA supports store and forward mode for maximum performance and cut-through mode for lower latency.

Integrated 1000BASE-X PCS

The Integrated 1000BASE-X PCS is 802.3 compliant and UNH tested, it integrates 8b10b encoding/decoding and auto-negotiation with the link partner for information exchange. GEM supports full and half duplex modes at 10/100M and full duplex at 1Gbps interface speeds for all popular media independent interface (MII) options including MII, RMII, GMII, RGMII, SGMII, QSGMII and TBI. An MDIO interface is supported for PHY management.

Availability

The MAC IP is available with various interface options and features:

Speed	Interface	Features
10/100Mbps	RMII, MII	
10/100M/1G	SGMII	
10/100M/1G	SGMII	TSN/AVB, PCS, DMA, 1588

Related Products

- Cadence VIP for Ethernet
- 1000BASE-X PCS for Ethernet

Deliverables

- Verilog HDL source code
- Cadence® Encounter® RTL Compiler synthesis scripts
- Datasheet and user guide with full programming interface, parameterization instructions, and synthesis instructions
- IP-XACT RDL generated address map
- Firmware core and Linus driver package
- Verilog testbench

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