VIP Datasheet

Simulation VIP for Ethernet 400G

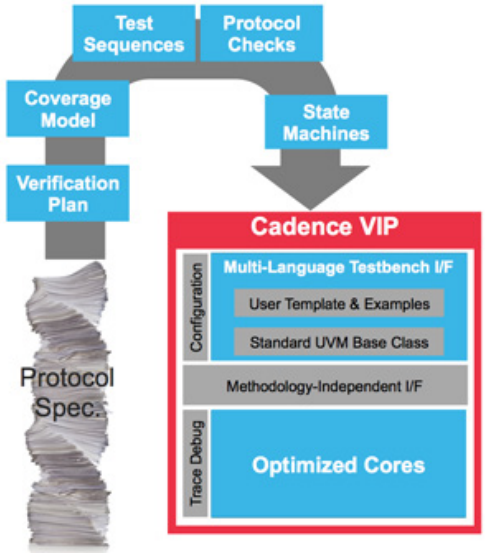
Supports Energy Efficient Ethernet (EEE)

Overview

Cadence® Simulation VIP is the world's most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.



Specification Support

This VIP supports IEEE P802.3bs_D1.4 for 400G and 200G, 25 Gigabit Ethernet Consortium specification and IEEE802.3by_D2p0. Ethernet specifications are developed and maintained by IEEE.

Product Highlights

- Supports speed of operations from 10 Gbps to 400Gbps
- Supports Energy Efficient Ethernet
- Supports Priority Flow Control
- Supports Physical Medium Attachment layer with both NRZ and PAM4 encoding
- Supports Forward Error Correction for both Fireside and Reed-Solomon

Supported Design-Under-Test Configurations

☑ MAC	☑ PHY	☐ Hub/Switch
☑ Full Stack	☐ Controller-only	☐ PHY-only

Deliverables

People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:

- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the "raw" coverage model results back to the protocol specification.

Key Features

- Link level flow control for each Class of Service (CoS) as defined by IEEE P802.1p
- Flow control mechanism in which overwhelmed network element sends a Pause frame which halts the transmission for a specified period of time.
- FEC appends to the Ethernet frame additional data that is a result of set of non-binary arithmetic functions performed on the data of the Ethernet frame. This additional data (known as the FEC parity octets) is used to correct errors at the receiving end of the link that may occur when the data is transferred through the link.
- EEE is a set of enhancements to the twisted-pair and backplane Ethernet family of computer networking standards that allow for less power consumption during periods of low data activity, per Standard IEEE 802.3az. (Clause 78)
- Management Data Input/Output(MDIO) serial bus defined for Ethernet family PHY's registers read and write.
- Custom VLAN,CRC, Length, Preamble, Proprietary Header supported through callback mechanism.
- Auto-negotiation for Ethernet backplane interfaces (Clause 73)
- Active, Passive configuration, Internal/External Clock modes, Full stack mode (MAC + PCS+FEC(RS or CL74) +PMA) or a valid combination of sub-layers (MAC only, MAC+PCS+PMA, PCS+FEC (RS or CL74) +PMA, FEC(RS or CL74) +PMA, PMA only). These can be used with(out) AN or PMD Link Training.
- 802.3, JUMBO, PAUSE, PFC-PAUSE, VII, Double tagged(S-VLAN tag and Q-VLAN tag) frame types
- 10 Gbps, 20Gbps, 25Gbps, 40Gbps, 50Gbps and 100Gbps,200Gbps(new),400Gbps
- PMD link training as described in Clause 72, Clause 93 of IEEE 802.3
- PCS: Clause 49, 82, 107,119
- PMA: Clause 48, 83, 109,120
- Fire code FEC (Clause 74), RS-FEC (Clause 91, 108)
- Support for MAC, MAC+PCS+PMA,PCS+PMA layer for 400G.
- Support for combined (PCS+FEC) as per Clause 119 for 400G
- Support for PMA with NRZ, PAM4 for 400G.
- Support for MAC, MAC+PCS+PMA,PCS+PMA layer for 200G.
- Support for combined (PCS+FEC) as per Clause 119 for 200G
- Support for PMA with NRZ, PAM4 for 200G.
- FEC Degrade feature as per IEEE P802.3bs_D1.4 Clause 119 for 400G and 200G.

Related Products

- Ethernet Simulation VIP
- Ethernet 25G Simulation VIP
- Ethernet Accelerated VIP
- Ethernet 40G/100G Simulation VIP

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