Simulation VIP for SPI

Overview
Cadence® Simulation VIP is the world’s most widely used VIP for digital simulation. Hundreds of customers have used Cadence VIP to verify thousands of designs, from IP blocks to full systems on chip (SoCs).

The Simulation VIP is ready-made for your environment, providing consistent results whether you are using Cadence Incisive®, Synopsys VCS®, or Mentor Questa® simulators. You have the freedom to build your testbench using any of these verification languages: SystemVerilog, e, Verilog, VHDL, or C/C++. Cadence Simulation VIP supports the Universal Verification Methodology (UVM) as well as legacy methodologies.

The unique flexible architecture of Cadence VIP makes this possible. It includes a multi-language testbench interface with full access to the source code to make it easy to integrate VIP with your testbench. Optimized cores for simulation and simulation-acceleration allow you to choose the verification approach that best meets your objectives.

Specification Support
The SPI VIP supports the following specifications:
- Samsung SPI based on the Exynos 5250 spec Revision 1.00
- Motorola SPI based on Block Guide V03.06

Supported Design-Under-Test Configurations
- Master
- Slave
- Hub/Switch
- Full Stack
- Controller-only
- PHY-only

Deliverables
People sometimes think of VIP as just a bus functional model (BFM) that responds to interface traffic. But SoC verification requires much more than just a BFM. Cadence Simulation VIP components deliver:
- State machine models incorporate the subtle features of state machine behavior, such as support for multi-tiered, power-saving modes
- Pre-programmed assertions that are built into the VIP to continuously watch simulation traffic to check for protocol violations.
- Test suites are provided for most Cadence VIP components.
- Pre-programmed coverage models used to capture interesting combinations of simulation results. By analyzing the results collected by the coverage model, engineers can tell if the simulations have exercised the various modes of operation of an interface.
- Verification plans for most protocols link the “raw” coverage model results back to the protocol specification.
Key Features

- Simultaneous transfer from master and slave.
- Supports 8/16/32-bit shift register for Tx/Rx.
- Supports 8-bit/16-bit/32-bit bus interface.
- Supports two independent 32-bit wide transmit and receive FIFOs.
- Supports Master-mode and Slave-mode.
- Supports Receive-without-transmit operation.
- Supports Slave select output.
- Supports mode fault error flag with CPU interrupt capability.
- Supports serial clock with programmable polarity and phase.
- Supports control of SPI operation during wait mode.

Test Suite

This VIP includes a basic test suite capability that includes:

- Constrained-random example tests
- 3rd party simulator test execution