Design IP Brochure

Slave Controller IP for MIPI I3C

Overview

Rapidly increasing numbers of sensors creates new design challenges for mobile, automotive, and Internet of Things (IoT) devices. These design challenges include significantly higher signal count and increased bandwidth requirements. To address these challenges the MIPI® Alliance has defined the I3C℠ interface for connecting all the sensors in a system.

The Cadence® IP Family for MIPI Protocols delivers area-optimized interface IP with the low power and high performance required for today's leading-edge devices. One member of this family is the Cadence Slave Controller IP for MIPI I3C.

Compliant with the latest MIPI I3C specification and legacy compatible with I2C℠, the Controller IP is engineered to quickly and easily integrate into any mobile embedded system on chip (SoC) device and expand sensor communication capabilities with better power efficiency.

Developed by experienced teams with industry-leading domain expertise, verified by silicon-proven and mature I2C IP and validated on a FPGA platform to reduce risk for designers, the IP will connect seamlessly to the Controller IP.

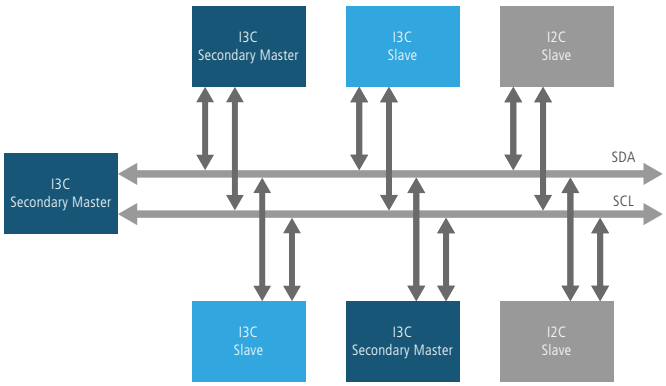

Figure 1: Example System-Level Block Diagram

Benefits

- Full-featured and highly configurable IP core that is area-optimized for each application
- Complete solution—complementary master/slave IP
- Fully verified on FPGA

The Controller IP is part of the comprehensive Cadence Design IP portfolio comprised of Interface, Memory, Analog, System and Peripheral IP.

Key Features

- Support for multiple transmission modes: Single Data Rate (SDR) and High Data Rate (HDR)
- Support for in-band interrupts, hot-join, peer-to-peer request, mastership request
- Compliant with the latest I3C specification
- I2C legacy device support
- Support for I3C common command codes
- APB interface support for register access
- Dynamic address assignment (DAA) support
- Command queue support
- Optional support for user generic I/O signal registers
- Interconnect protocol

Product Details

The Controller IP is compliant with the MIPI Alliance I3C sensor specification for embedded systems applications enabling the incorporation of more sensors in a device. This is a soft IP ideally suited for implementation in ASIC SoC designs with increasing numbers and types of sensors. It provides reduced energy consumption and higher performance over legacy designs.

Architecture

The Controller IP consists of three major modules: slave bus controller, common command codes (CCC) controller and frame generator.

HDR-DDR Mode

The slave device supporting HDR-DDR implements the APB interface and provides a simple payload control mechanism FIFO for the read and write data.

The HDR-DDR data payload FIFO will be accessible using the APB register interface so the firmware can perform a single read address access to the FIFO for each packet of data and cyclic redundancy check (CRC) received, and a single address write to the FIFO for data, payload and CRC for any master HDR-DDR read transaction.

The firmware will be responsible for reading and checking the received DDR data, and also forming the 20-bit packet for the transmitted data including structure for the data payload and CRC packet.

General Purpose Registers

The IP allows the configuration to control the addition of user defined registers. The registers map to general purpose input (GPI) and output (GPO) signals at the top level or for static information.

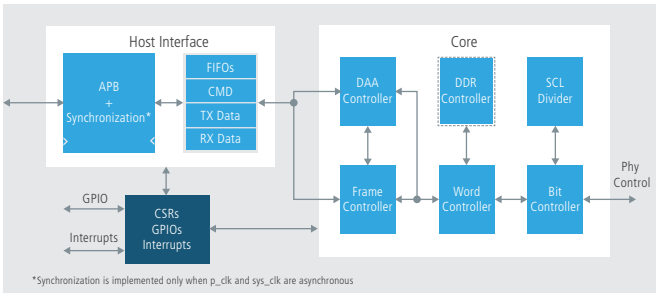

Figure 2: IP-Level Block Diagram

The GPI and GPO registers support read or write transaction access using an I3C single register address-I3C private read and write messages. The maximum number of GPI and GPO messages is 256.

Clock Domains

The I3C bus clock is the main clock for the IP for MIPI I3C Slave IP. The bus controller and CCC controller modules are running on this clock. For example, the serialization and deserialization logic, all the PHY control signals and all CCC registers are launched and captured on this clock.

The whole frame controller works on the system side clock. For example, GPIs and GPOs, Bus free and idle counter are launched and captured on this clock.

Configurations Options

- FIFO (RX and TX FIFO depth)
- Secondary master support
- HDR-DDR mode enable/disable
- Command queue depth
- I3C devices that can reside on the I3C Bus with maximum number

Related Products

- Cadence Simulation VIP for MIPI I3C
- Cadence IP for MIPI I3C Master Controller
- Cadence IP for MIPI I2C Controller
- Cadence Verification IP for MIPI SoundWire℠

Deliverables

- Documentation—Integration guide, user guide, and release notes
- Clean, readable, synthesize-able Verilog RTL
- Synthesis scripts
- Sample verification testbench with integrated BFM, monitors, and sanity tests

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