Overview

Today's leading-edge mobile devices contain increasingly integrated functionality that enables growing volumes of content and video, more ways to control and interact, and longer battery life. The MIPI® Alliance defines semiconductor standards that support growing complexity and reduce device form factor. The Cadence® family of interface IP for MIPI protocols is leading the way with mobile-optimized low power and high performance. Compliant with the MIPI Specification for M-PHY® with speeds up to 2.9Gbps per lane, the Cadence Design IP for MIPI M-PHY for TSMC also supports CSI-3, LLI, and SSIC IP.

Developed by experienced teams with industry-leading domain expertise and extensively validated by multiple hardware platforms, the M-PHY IP is silicon-proven and shipping in high volume in multiple mobile devices. The M-PHY IP is engineered to quickly and easily integrate into any design, and to connect seamlessly to a Cadence, or third-party, Reference M-PHY MODULE Interface (RMMI) compliant controller. Implemented on several popular semiconductor processes, the M-PHY IP provides a cost-effective, low-power solution for demanding mobile applications.

The IP is a mixed-signal PHY consisting of an M-PHY transmitter and an M-PHY receiver. The Cadence IP is developed and validated to reduce risk for designers so that their system on chip (SoC) can be first-time right. Developed and available early in the lifecycle of the most advanced semiconductor process nodes, the M-PHY IP is designed to be robust under varying signal strength and noise conditions.

The M-PHY IP is part of the comprehensive Cadence Design IP portfolio comprised of interface, memory, analog, and systems and peripherals IP.

Key Features

- Compliant to MIPI Specification for M-PHY v2.0
- Integrated BIST capable of producing and checking PRBS, CRPAT, and CJTPAT
- Scalable up to four LANEs per SUB-LINK
- Configurable as Type-I or Type-II MODULE
- Internal and external data-path loop-back modes
- Standard RMMI interface
- Matched analog design for low LANE-to-LANE skew and maximum timing margins
- Mobile-optimized area and power
- Receiver supports terminated/unterminated operation
- Slew-rate control for reduced EMI

Benefits

- Proven design in volume production
- Scalable LANE module offer great SoC flexibility
- Extensive testability enable low risk development and fast TTM
Product Details

The M-PHY IP is a mixed-signal design that uses optimized and matched analog design for reducing LANE-to-LANE skew and maximizing timing margins. The full support of HS Gears with both Rate A and B, and Low-Speed signaling (LS-mode) provides great flexibility to further scale bandwidth to application needs.

PHY Architecture

The M-PHY IP employs modular implementation with scalability for up to four lanes in one sub-link. It provides excellent control over floor planning, placement and I/O integration while maintaining reliability and ease-of-use of the IP macro.

Controller Interface

The Controller Interface implements the RMMI found in Annex A of the specification for M-PHY. RMMI supports controllers based on MIPI CSI-3, and LLI, and SuperSpeed USB Inter-Chip (SSIC) specifications.

Transmitter and Receiver (M-TX and M-RX)

When configured as a Type-I module, the M-PHY IP supports both high-speed (HS-MODE) and low-speed (LS-MODE) signaling. Transfer speeds up to 2.9Gbps per lane (HS-G2) are supported. PWM-BURSTS for low-power, low-speed operation (PWM-G1 to PWM-G5) are also supported.

As a Type-II MODULE, the IP also supports HS-MODE and LS-MODE signaling. HS-MODE transfer speeds for a Type-II MODULE are the same as for a Type-I MODULE, while LS-MODE signaling uses SYS-BURSTS rather than PWM-BURSTS.

Availability

The M-PHY IP is available at various process nodes and protocols, including:

<table>
<thead>
<tr>
<th>Speed (Gbps)</th>
<th>Protocol</th>
<th>Process</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.9</td>
<td>M-PHY Gear 2</td>
<td>TSMC 28HPM</td>
</tr>
<tr>
<td>2.9</td>
<td>M-PHY Gear 2</td>
<td>TSMC 28HPC</td>
</tr>
<tr>
<td>2.9</td>
<td>M-PHY Gear 2</td>
<td>TSMC 28HPL</td>
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</tbody>
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Deliverables

- GDS II macros with abstract in LEF
- Verilog post-layout netlist
- STA scripts for use at chip or standalone PHY levels
- Liberty timing model
- SDF for back-annotated timing verification
- Verilog models of I/O pads and RTL for all PHY modules
- Verilog testbench with memory model, configuration files, and sample tests
- Complete technical documentation set
- Verification IP set up files

Related Products

- Design IP for MIPI D-PHY™, SoundWire™ Master Controller, SoundWire Slave Controller, CSI-2™ Receiver, CSI-2 Transmitter, DSI Transmitter, SLIMbus® Device Controller, SLIMbus Manager Controller

The Design IP for MIPI M-PHY is part of the comprehensive Cadence Design IP portfolio comprised of interface, memory, analog, and systems and peripherals IP.

For more information, visit ip.cadence.com