

# Slave Controller IP for MIPI SoundWire

## Overview

Today's leading-edge mobile devices increasingly integrate functionality that enables growing volumes of audio and video, more ways to control and interact, and longer battery life. The MIPI® Alliance defines semiconductor standards for mobile devices that support growing complexity and reduced device form factor.

The Cadence® IP Family for MIPI Protocols delivers area-optimized interface IP with the low power and high performance required for today's leading-edge devices. One member of this family is the Cadence Slave Controller IP for MIPI® SoundWire<sup>SM</sup> v1.1, providing low-cost, low-power connectivity for audio data transport and control.

Developed by experienced teams with industry-leading domain expertise and extensively validated with multiple hardware platforms, the Controller IP is engineered to quickly and easily integrate with SoundWire Master IP controllers.

The Controller IP is part of the comprehensive Cadence Design IP portfolio comprised of interface, memory, analog, and system and peripheral IP.

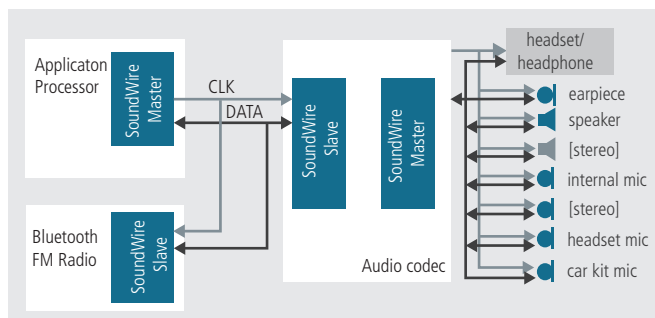


Figure 1: Example System-Level Block Diagram

## Benefits

- Superior power and performance compared to other established audio connectivity standards
- Complete solution—complementary master also available
- Optimized for both SoC and Peripheral applications

## Key Features

- MIPI compliant slave controller with multi-lane capability
- APB Slave interface for control port and master configuration registers
- APB Master interface for external user defined registers
- Support for Full, Reduced and Simplified Data Ports
- Configurable Data Ports with user-programmable features
- Isochronous, TX- or RX-controlled, or fully asynchronous transport
- Support for both PDM and PCM audio formats
- Single clock operation and clock gating support for low power

## Product Details

The Controller IP provides standard-based IP with multi-lane capability shown in Figure 2. It is designed to provide low-cost, low-power connectivity for audio data transport and control. SoundWire interface is utilized to provide two types of connectivity. The first carries PCM audio data between a mobile application processor and a standalone audio codec or Bluetooth®/FM radio controller. The second type carries PDM audio between the audio codec and MEMS microphone or speaker amplifiers.

## Register Access

There are 2 sets of control registers. Standard registers are accessed via SoundWire interface while IP specific registers are accessed via APB slave interface to allow local firmware to control the device. All registers are mapped to host memory space. Certain timing critical registers are banked to allow synchronous switching without interruption to data streams. It can operate in a self contained manner without local firmware support. Hardware-based device enumeration logic supports autonomous operation so that once the device is attached to the SoundWire interface, it automatically synchronizes to the SoundWire Master and is ready for enumeration.

## Control Port

The control port function supports READ/WRITE/PING commands received from the SoundWire interface. It can assert PREQ based on the following events: frame parity error, bus clash, data port overflow/underflow, test fail, asynchronous wake-up and user defined interrupts.

## Data Port

The slave controller supports configurable numbers (1 to 14) of physical data interface (PDI); each PDI can be configured as TX direction or RX direction. The PDI FIFO has configurable width from 1 to 32 bits, and depth of 4 to 32 entries, synchronous or asynchronous.

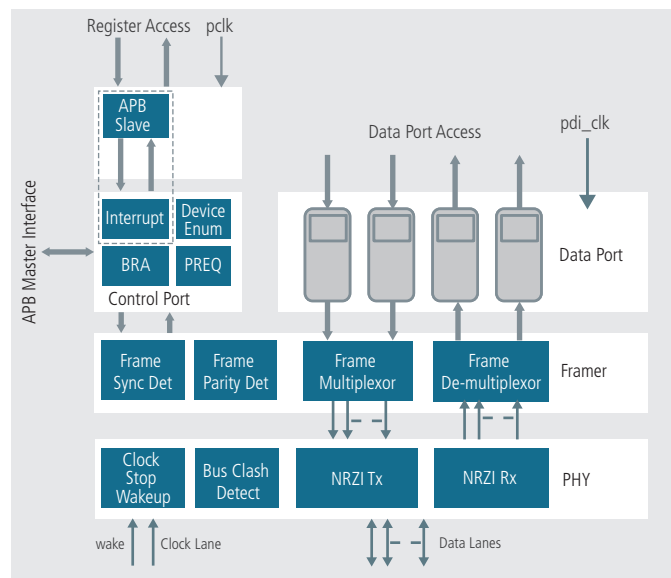


Figure 2: IP-Level Block Diagram

## Frame Transport

The slave controller supports isochronous, TX-controlled, RX-controlled and fully asynchronous transport modes and standard-based frame parameters: offset and sub-frame offset, Hstart and Hstop, sample interval, BlockPackingMode, BlockGroupCount, LANESelect.

## Digital PHY Interface

The IP provides standard interface to the external PHY module with data enable, bus keeper enable signals, and slew rate control output.

## Related Products

- Cadence Master Controller IP for MIPI SoundWire 1.1
- Cadence Tensilica® HiFi DSP for Audio
- Cadence Manager Controller IP for MIPI SLIMbus®
- Cadence Device Controller IP for MIPI SLIMbus
- Cadence Design IP for I2S Single Channel (I2S-SC) Bus Controller
- Cadence Design IP for I2S Multi Channel (I2S-MC) Bus Controller
- Cadence Controller IP for Sony/Philips Digital Interface Format (S/PDIF)

## Deliverables

- Documentation—implementation specification, user guide, release history
- Clean, readable, synthesizable Verilog RTL
- Synthesis scripts
- Sample verification testbench with integrated BFM, monitors, and sanity tests

For more information, visit [ip.cadence.com](http://ip.cadence.com)

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