VIP Datasheet

Accelerated VIP for USB 2.0

Overview

Sometimes chips are just too big to verify with logic simulation software. SoCs comprised of tens of millions of logic gates will bog down software simulators, even when running on the fastest servers.

Simulating big designs requires hardware-assisted verification, an approach that uses special-purpose hardware, like Cadence® Palladium® XP systems, to dramatically boost simulation performance.

Just as simulation VIP simplifies traditional logic simulation, accelerated VIP makes hardware-assisted verification easier and more productive.

Cadence Accelerated VIP includes the same multi-language testbench interface provided with the simulation VIP as well as acceleration-optimized cores. This combination enables two popular methods of hardware-assisted verification: simulation acceleration and embedded testbench.

Specification Support

The USB 2.0 AVIP is based on the USB 2.0 specification

Usage Options

- [x] Simulation Acceleration
- [ ] Embedded Testbench

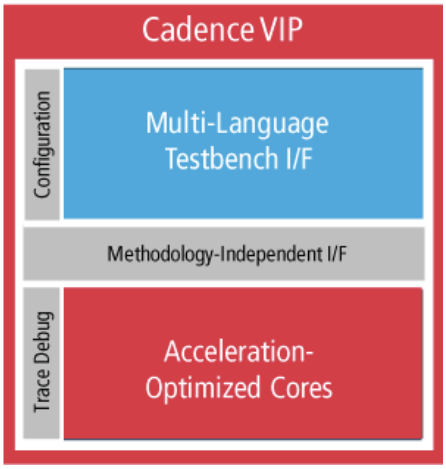
Supported Design-Under-Test Configurations

- [x] Master
- [x] Slave
- [ ] Hub/Switch
- [x] Full Stack
- [ ] Controller-only
- [ ] PHY-only

Product Highlights

The USB 2.0 AVIP supports the following features:

- Control transfer
- Bulk transfer
- Low power management



The USB 2.0 AVIP supports the following testbench interfaces:

- SV-UVM
- C++

Supported flows:

- Simulation acceleration with Palladium XP, compiled using the IXCOM flow

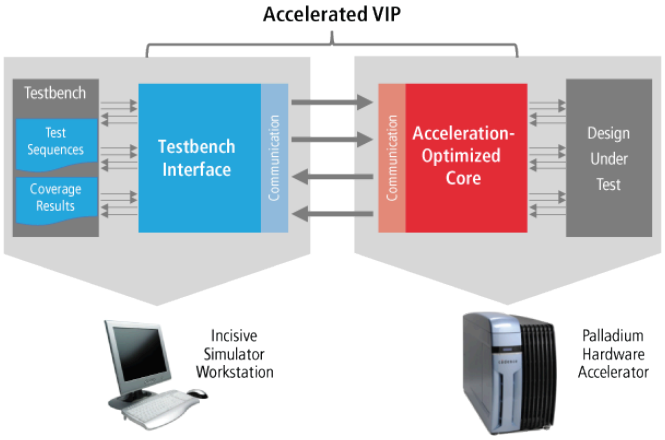
Key Verification Capabilities

- 8/16-bit UTMI+ interface
- The signal-level interface is connected via a UTMI+ interface to the DUT
- Control and bulk transfers
- Full-Speed, Hi-Speed data transfer in both Host and Device modes
- Configurable for up to 15 IN and 15 OUT endpoints
- Logs transactions in a log file and logging control
- Stimulus access to received transactions using callbacks
- Low power management
- Device Firmware Upgrade (DFU) capability (USB 2.0 AVIP Host only)

Simulation Acceleration

In simulation acceleration, the Cadence Palladium XP system works in conjunction with the Cadence Incisive® Simulator to divide up the simulation task. The Palladium XP runs the design under test while the Incisive simulator runs the testbench. Accelerated VIP is inserted for each of the standard interfaces in the design with the testbench interface running on Incisive and the acceleration-optimized core running on the Palladium XP.

Most of the testbench components employed in simulation can be reused, which saves set-up time and preserves the controllability and observeability of traditional logic simulation. With this approach, performance is often up to 1000X faster than logic simulation.



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