Tensilica’s Xtensa® LX processor is the only processor core for system-on-chip (SOC) designs that provides the I/O bandwidth, compute parallelism, and low-power optimization equivalent to hand-optimized, RTL-designed non-programmable hardware blocks. With Tensilica’s unique automated processor generator, every Tensilica® customer is able to quickly generate a tailored version of the Xtensa LX processor optimized for their particular application, Ideal for handling traditional SOC embedded processor control tasks as well as compute-intensive datapath hardware tasks, the Xtensa LX processor is the new basic building block for complex SOC design.

The configurable, extensible and synthesizable Xtensa LX processor core is unlike any other conventional embedded processor or DSP core. Using the Tensilica technology, the SOC designer can mold one or more Xtensa LX processor to an exact fit to the target task. The designer selects and configures predefined processor attributes and, using the Tensilica Instruction Extension (TIE) methodology, adds Verilog-like descriptions of execution datapaths, I/O ports and registers that can deliver performance, area, and power characteristics equivalent to custom logic design. Or, the designer can use the XPRES Compiler to analyze the C algorithm and automatically suggest configuration options and extensions that will run that algorithm orders of magnitude faster. Compared to traditional hardware design, Xtensa LX processors deliver similar quality of results with the added benefits of accelerated design time and post-silicon software programmability, making Xtensa LX processors ideal choices for all complex SOC designs.
Figure 1: The Xtensa LX architecture starts with base ISA features common to all Xtensa LX cores. SOC developers can configure the Xtensa LX processor from a menu of predefined options, and add functional units of their own design to optimize algorithm performance, achieving specifications equivalent to hand coded custom logic blocks in a fraction of the time.
Feature Summary

Tensilica’s processor generator technology creates a complete RTL hardware description of a customized Xtensa LX processor, plus a comprehensive suite of software development tools, EDA implementation scripts, and system models – all in about 1 hour.

Optional Pre-defined Execution Units

• 32-bit multiplier
• 16-bit MAC
• 4-way SIMD Vectra™ LX DSP engine
• Floating point unit

Configurable Interface Options

• Designer-defined I/O ports up to 1M wires
• Optional processor interface (PIF) to system bus, choice of 32, 64 or 128-bit width with in-bound DMA [slave mode] option
• Optional high-speed Xtensa Local Memory Interface (XLMI)
• Write Buffer: selectable from 4 to 32 entries
• Optional second data Load/Store unit

Sea of Processors / Multiple Processor Design Support

• System modeling capability: optional Xtensa Modeling Protocol (XTMP) simulation environment
• Multiple-processor on-chip debug capable with break-in/out control
• Optional processor ID interface and special register
• Memory synchronization and conditional store instruction option provides support for memory semaphore operations and the release consistency model of memory-access ordering

Complete Hardware Implementation and Verification Flow Support

• Automatic generation of RTL and tailored EDA scripts for leading edge process technologies, including physical synthesis and 3D extraction tools
• Auto-insertion of fine-grained clock gating delivers ultra-low power
• Hardware emulation support including automated FPGA netlist implementation
• Comprehensive diagnostic test bench
• Formal verification support for designer-defined functionality

High-speed, High-accuracy System Simulation Models Automatically Created for Each Configuration

• Pipeline-modeling, cycle-by-cycle accurate Xtensa instruction set simulator
• Multiple-processor simulation with XTMP option
• Hardware-software co-verification model for Mentor Seamless

Comprehensive Development Environment and Software Tool Support

• Xtensa Xplorer™ development environment accelerates the analysis and development of Xtensa LX processor cores and SOCs designed with multiple Xtensa LX processors
• Sixth generation Xtensa Tools development suite automatically configured for each processor, including the advanced Xtensa C/C++ compiler (XCC)
• OSKit™ overlays provide automatic support of Mentor/ATI’s Nucleus and Wind River Systems VxWorks for Tornado operating systems

XPRES Compiler Support

• Automated configuration synthesis from C/C++ source code, no modification required

Performance Summary

Processor Architecture

• High-performance 32-bit RISC with designer-selectable 5-stage or 7-stage pipeline
• Optional FLIX (Flexible Length Instruction Xtensions) designer-defined, highly parallel instruction extensions. Parallelism of designer-defined execution units: 2-wide to 15-wide.

Instruction Set

• Xtensa ISA with compact 16-bit and 24-bit base instruction set and optional designer-defined 32-bit or 64-bit FLIX instructions.

<table>
<thead>
<tr>
<th>Area</th>
<th>Clock Rate</th>
<th>Power Dissipation</th>
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<td>Optimized for area</td>
<td>130nm LV process. Worst case conditions, Optimized for speed</td>
<td>130 nm LV process speed-optimized netlist under typical operating conditions</td>
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<td>RTOS-ready base configuration, 5-stage</td>
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<td>350MHz</td>
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<td>Performance optimized task engine, 7-stage, no PIF</td>
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<tr>
<td>Minimum configuration</td>
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**SOC Design Methodology**

SOC design can provide higher performance, lower cost, smaller form factor and longer battery life through lower power. But SOC designers often experience design bottlenecks in block-level integration and verification, hardware/software co-development and semiconductor portability. Until recently, embedded SOC designers have had to develop solutions based around rigid processor cores that were designed for workstation architectures, and augment those cores with large amounts of custom logic. The Xtensa LX solution provides a configurable microprocessor core that handles not only conventional processor tasks, but is easily augmented to deliver the performance and power of custom logic. The Xtensa LX processor is quickly integrated with other system blocks and is easily adapted to the needs of today’s high volume, high-performance embedded applications.

**Post-RISC Processor Core**

The Xtensa LX 32-bit architecture features a compact instruction set optimized for embedded designs. The base architecture has a 32-bit ALU, up to 64 general-purpose physical registers, 6 special purpose registers and 80 base instructions, including improved 16- and 24-bit (rather than 32-bit) RISC instruction encoding. The Xtensa LX implements the proven Xtensa instruction set architecture (ISA), which enables designers to achieve significant code size reductions compared to conventional RISC cores. Reducing code size results in higher performance and better power dissipation – key to saving cost in highly integrated SOC designs. The Xtensa ISA’s 16-and 24-bit encoding also provides powerful branch instructions and zero-overhead loops, and bit manipulations including funnel shifts and field-extract operations.

**Rapid Design Exploration**

The Xtensa Processor Generator and the Xtensa Xplorer development environment assist SOC designers in creating tailored, application-specific embedded processors quickly and reliably. Designers with existing application software code can profile the application, identify hot spots, add new instructions and execution units to optimize performance and regenerate a new processor – all within a matter of hours.

Hardware designers with a reference specification can quickly design execution unit semantics with the desired datapath characteristics, add new I/O ports of nearly unlimited complexity to stream data into the new execution unit datapaths, add new instructions to the processor, and write simple C programs to test the new processor – all from within the integrated Xtensa Xplorer design environment.

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**Figure 2:** Every instance of the Xtensa LX processor includes comprehensive hardware, software and system modeling deliverables – all automatically generated by Tensilica’s Xtensa Processor Generator.
Highly Configurable Base Processor Feature Set

Via the Xtensa Xplorer design environment, the Xtensa Processor Generator allows quick configuration of many Xtensa LX core preconfigured options, including:

Execution Unit and ISA Options

- Multipliers: 32- or 16-bit
- DSP engines
  - Single 16-bit MAC
  - 4-MAC SIMD Vectra LX DSP engine
- Floating point unit
- Multiple-processor synchronization instruction set option

Interface Options

- Processor interface (PIF)
  - Width: 32/64/128-bit
  - Optional “no PIF” configuration
  - Inbound DMA option
- XLMI high-speed local interface
- Choice of 1 or 2 general purpose load/store units
  - Enables classic X-Y style DSP configurations
- Big-Endian/Little-Endian byte ordering
- On-chip debug port
- Trace port signals
- Up to 32 interrupts
- Designer-defined queues/ports
  - Up to 1024 logical ports
  - Up to 1024 pins per port

Memory Subsystem Options

- Local data and instruction caches
  - Up to 4-way set associative
  - Up to 32 KB
  - Write-back and write-through cache write policy
- Separate local RAM, ROM areas for data, instructions up to 256Kbytes each

Design Support

- Pipeline-modeled, cycle-accurate instruction set simulator and Xtensa Modeling Protocol (XTMP)
- Hardware/software co-verification model for Mentor Graphics’ Seamless
- RTOS support packages for ATI Nucleus and WindRiver® Systems’ VxWorks®

Processor Extensions – Accelerating Processor Performance to Custom Logic Design Levels

The Tensilica Instruction Extension (TIE) language is used to describe new instructions, new registers and execution units, and new I/O ports that are then automatically added to the Xtensa LX processor. TIE is a Verilog-like language used to describe desired instruction mnemonics, operands, encoding and execution semantics. TIE files are inputs to the Xtensa Processor Generator. The Generator automatically builds a version of the Xtensa LX processor and the complete tool chain that incorporates the new TIE instructions.

FLIX Architecture – Highly Parallel Implementations

The Xtensa LX implements Tensilica’s FLIX (Flexible Length Instruction Xtensions) architecture. FLIX is a configuration option that allows designer-defined instructions to consist of multiple, independent operations bundled into a compact 32-bit or 64-bit instruction word. Wide 32/64 bit FLIX instruction formats are seamlessly and modelessly intermixed with the base Xtensa ISA’s existing 16/24 bit instructions – there is no mode switch penalty to utilize a FLIX instruction. The FLIX architecture allows the implementation of highly parallel processors with a range from 2 to 15 parallel execution units. Thus Xtensa LX can deliver the ultra-high performance characteristic of specialty ultra-wide instruction word processors, without the negative code size implications typically found in such VLIW or ULIW solutions. In fact, Xtensa LX processors with FLIX can often deliver higher performance and smaller code size at the same time. This performance increase comes with very little overhead – adding only 2,000 gates to the size of the processor for instruction decode and control.

Ports and Queues – Unlimited I/O Bandwidth

The FLIX architecture also enables a fundamental breakthrough in embedded processor design – designer-defined I/O ports. Simple one-line declarations [see Figure 3] in a TIE file define new I/O ports for configurations of Xtensa LX processors. These new ports are used as direct connections to other logic within an SOC or to other Xtensa LX processors. TIE Ports and TIE Queues move data into/out of an Xtensa LX processor without the conventional processor overhead of a load or store operation.
TIE Queues enable Xtensa LX processors to have virtually unlimited I/O bandwidth. TIE input Queues present a familiar pop/empty/data interface to the external logic, while TIE output Queues present a similar push/full/data interface. All interactions with the Xtensa LX processor pipeline, including pipeline control and speculation handling, are automatically implemented by the processor generator. As figure 3 illustrates, the SOC designer need only specify a handful of commands to create a high-bandwidth set of I/O Queues and execution units that operate on those Queues.

A maximum of 1024 logical Ports, each consisting of up to 1024 pins, can be added to each configuration of an Xtensa LX processor. TIE Ports and Queues can be utilized every clock cycle without the use of load/store instructions – providing virtually unlimited I/O bandwidth for an embedded Xtensa LX core.

**Figure 3:** An example of designer-defined I/O Queues and an execution unit that performs 2 operand inputs, one operand output, and a 256-bit Add in a single instruction.

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**Better Interfaces to On-Chip Memories**

To address the growing speed disparity between standard cell logic and memories (memory access speeds have not scaled as well as logic in the migration from 180 nm to 130 nm and now 90 nm), the Xtensa LX processor features a configurable pipeline. Designers can select a configuration option that adds two additional clock cycles for memory access if required by the application. While the Xtensa LX processor’s standard 5-stage pipeline is very efficient for many applications, designers employing large local memories or specialized low-power memories with longer access times will find advantages in moving to a longer pipeline, resulting in a higher system clock frequency.

**Performance and I/O of Hard-wired Logic, Without Risky State Machines**

The combination of TIE Ports and Queues with parallel FLIX execution units implemented in an Xtensa LX processor allows SOC designers to achieve virtually the same levels of inter-block I/O bandwidth and intra-block computational parallelism as with hard-wired logic designed with traditional RTL design methodologies. But unlike RTL-based design, configured and extended Xtensa LX processors are pre-verified by the Xtensa Processor Generator, and do not require hard-wired implementation of complex state machines. Instead of state machines, the complex datapaths added to Xtensa LX cores are sequenced/controlled by the instruction stream of the Xtensa LX processor. That means the “control logic” is fully software programmable and debuggable – reducing verification time and risk for the entire SOC.
Ideal for Applications Where Low Power is Critical

Clock gating is a very effective power reduction technique that shuts down power to parts of the logic that are not in use on a particular clock cycle. Tensilica has automated the insertion of fine-grained clock gating for every functional element of the Xtensa LX processor including functions conceived of and created by the designer. This automation gives the Xtensa LX a significant advantage over RTL design, where manual, error-prone post-layout tuning of clock circuits is often required.

The Xtensa LX processor’s new architecture dramatically lowers power consumption in large configurations with many designer-defined functions. But even without the inclusion of designer-defined functionality, the Xtensa LX processor is designed to use power very efficiently. The minimum configuration of the Xtensa LX processor dissipates less than 50 µW/MHz in a representative 130 nm process technology.

Comprehensive and Automated Software Tool Support

Every Xtensa LX processor is automatically generated with a complete set of software development and modeling tools tailored to the exact Xtensa LX configuration. The Xtensa Tools suite includes the high-performance vectorizing Xtensa C/C++ compiler; the XPRES Compiler for automatically generating processor configurations from standard C/C++ code; a GNU-based assembler/linker/debugger/profile; the pipeline-modeled, cycle-accurate Xtensa Instruction Set Simulator; and Xtensa Modeling Protocol system simulation API. And all of the Xtensa development tools are tightly integrated within the Xtensa Xplorer development environment [see Figure 5], the only tool that integrates software development, processor optimization and multiple-processor SOC architecture tools into one common design environment.

Figure 4: Illustration of high-performance streaming data design using multiple designer-defined TIE Ports and Queues.

* Up to 1 million I/O pins