Diamond 388VDO Dual Core Video Decoder/Encoder

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Member of the Technical Staff
Diamond 388VDO Design Goals

- Video encode & decode up to
  - 720 x 480 @30 fps (NTSC)
  - 720 x 576 @25 fps (PAL)

- Support multiple coding standards @ main profile
  - H.264 main profile @ L3 decoder
  - MPEG-4 ASP [no GMC] @ L5 decoder
  - MPEG-2 MP @ ML decoder
  - WMV9/VC1 main profile decoder
  - MPEG-4 ASP encoder

- Programmable solution

- Less than 100MB/s memory bandwidth requirement for the decoder

- Operating frequency <200Mhz
  - Can be implemented in 130nm G technology
Video Decoder Performance Requirements

H.264 Main Profile decode cycle requirements on unaugmented Xtensa core

<table>
<thead>
<tr>
<th></th>
<th>Million Cycles/sec</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rugby CABAC 5.4Mbps</td>
<td>2518</td>
</tr>
<tr>
<td>Rugby CAVLC 5.4Mbps</td>
<td>1918</td>
</tr>
</tbody>
</table>
Video Decoder Data-Flow Path

Encoded Bitstream → Entropy Decode → $Q^{-1}$ → $T^{-1}$ → D → + → Motion Compensate → Inter Intra

Intra Predict

Previously Reconstructed Reference Frames

DeBlock Filter

Reconstructed Frame to Display

+ → D

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Two Types of Tasks in Video

**Sequential processing**
- Decode headers from bitstream
  - Control code
- Decode transform blocks from bitstream
- Decode and compute motion vectors
- Inverse quantization (optional)

**SIMD algorithms**
- Deblocking
- Motion compensation
- Inverse transform
- Inverse quantization (optional)
Tradeoffs Considered

How many cores?
• Profile the application on the Xtensa cycle-accurate ISS model for a variety of streams (bitrates, complexity)
• Estimate performance gains from ISA extensions for the different algorithms
• \( \Rightarrow \) Two cores minimum (@200Mhz clock frequency)

Homogeneous or heterogeneous?
• Video consists of two types of tasks that need different ISA extensions
• From profiles it was estimated that the cycles on both cores would be balanced
• \( \Rightarrow \) Two heterogeneous cores
**Design Approach**

- **Extend Xtensa ISA**
  - Generate instructions as general as possible
    - To support the multiple decode and encode standards
    - To support future codecs
  - Use 16- and 8-way SIMD
  - Combine basic operations into new instructions
  - Design new instructions using high-level Tensilica Instruction Extensions (TIE) descriptions

- **Design intelligent multi-channel DMA engine**
  - Hide external memory latency
  - Support DMA from external memory to a core and from core to core (instruction and data memory)
Stream Processor functions

- entropy decoding, transform block decoding, motion-vector decoding and calculation, control code)
- Set up reference DMAs using decoded motion vectors

Pixel Processor functions

- Deblocking, Motion Compensation, Inverse Transform, etc
- DMA reconstructed frames to external memory
Stream Processor configuration

- ISA extensions for sequential function acceleration
  - Fused instructions
  - 2- and 3-issue instructions
- 128b data memory/PIF width
- DMA path to both data/instruction memories
Pixel Processor configuration

- 8 and 16 way SIMD instructions for pixel processing acceleration
- External queue interfaces to transpose block
  - Transpose is a fast row-to-column exchange of an array
- DMA path to both data/instruction memories
- 128b data memory/PIF width
Context-adaptive binary arithmetic coding (CABAC) achieves higher compression in H.264

- Our solution: Xtensa ISA extensions
- Peak decode performance is one bin per cycle
- CABAC decoding of one 4x4 transform block:

<table>
<thead>
<tr>
<th></th>
<th>Millions of cycles per second</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unaugmented core</td>
<td>710</td>
</tr>
<tr>
<td>ISA extended core</td>
<td>13</td>
</tr>
</tbody>
</table>

- Area cost: 20K gates for CABAC ISA extensions
### ISA Extension Results: Profile Comparison

#### H.264 Main Profile decode of 5.4Mbps Rugby stream

<table>
<thead>
<tr>
<th></th>
<th>CABAC unaugmented</th>
<th>CABAC ISA extended</th>
<th>CAVLC unaugmented</th>
<th>CAVLC ISA extended</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Stream Processor</strong></td>
<td>1,300</td>
<td>174</td>
<td>701</td>
<td>168</td>
</tr>
<tr>
<td><strong>Pixel Processor</strong></td>
<td>1,218</td>
<td>178</td>
<td>1,217</td>
<td>162</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>2,518</td>
<td>352</td>
<td>1,918</td>
<td>330</td>
</tr>
</tbody>
</table>
H.264 Main Profile D1 Decode: Min Clock Rate vs Video Bitrate
388VDO Can Support Large Memory Latencies

- H.264 Main Profile decode of Mobile Calendar bitstream at 4.3 Mbps
VDO Encoder Block Diagram

1. Input Images
2. ME
3. DCT
4. Q
5. IDCT
6. Q-1
7. MC
8. Partial Decoder
9. Decoded Reference Images
10. Rate Control
11. VLE
12. Bitstream generation

Flow:
- Input Images → ME → DCT → Q → IDCT → Q-1 → MC → Partial Decoder
- Rate Control
- VLE
- Bitstream generation
MPEG-4 performance requirement:
- MPEG-4 Encode requires 4,895 MCPS on unaugmented Xtensa core

Most cycles spent in Motion Estimation

<table>
<thead>
<tr>
<th></th>
<th>Million of cycles required on unaugmented core</th>
</tr>
</thead>
<tbody>
<tr>
<td>16x16 SAD</td>
<td>527</td>
</tr>
<tr>
<td>Diamond</td>
<td>735</td>
</tr>
<tr>
<td>Half Pel</td>
<td>1,143</td>
</tr>
<tr>
<td>8pt SAD</td>
<td>1,659</td>
</tr>
<tr>
<td>Control</td>
<td>204</td>
</tr>
<tr>
<td>Total</td>
<td>4,268</td>
</tr>
</tbody>
</table>
Design goal:

Map 4.2 billion cycles into 120 million

Approach:

- 16 way SIMD for fast Sum of Absolute Difference (SAD) calculation
- Algorithm optimizations to remove unnecessary loading of data
- 3 operations per cycle (3-way FLIX)
- Optimize control flow with data flow
Fast, flexible and fully programmable
• Optimized with generalized Motion Estimation instructions
• Not specific just to current MPEG-4 encoder implementation

ISA extensions support:
• 16x16 pixel SAD calculation in 60 cycles
• Calculates up to four neighboring 16x16 SADs in 100 cycles
• Four 8x8 pixel SAD calculations in 60 cycles
• Progressive and interlace support
• Find best half pel around full pel in 300 cycles (8 SAD calculations on half pel grid)
## Motion Estimation Optimization Results

<table>
<thead>
<tr>
<th></th>
<th>Millions of cycles required on unaugmented core</th>
<th>Millions of cycles required on ISA extended core</th>
</tr>
</thead>
<tbody>
<tr>
<td>16x16 SAD</td>
<td>527</td>
<td>16.3</td>
</tr>
<tr>
<td>Diamond</td>
<td>735</td>
<td>8.4</td>
</tr>
<tr>
<td>Half Pel</td>
<td>1143</td>
<td>10.7</td>
</tr>
<tr>
<td>8pt SAD</td>
<td>1659</td>
<td>14.2</td>
</tr>
<tr>
<td><strong>Motion Estimation</strong></td>
<td><strong>4268</strong></td>
<td><strong>76.2</strong></td>
</tr>
</tbody>
</table>

### Area:

Less than 40Kgates for all Motion Estimation extensions
Encoder performance

Cycle requirement: 188Mcycles/sec
  - 4.8Bcycles/sec reduced to 376Mcycles/sec

Quality comparison between 388VDO and Momusys Reference encoder

<table>
<thead>
<tr>
<th></th>
<th>Encoding PSNR difference (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max degradation</td>
<td>0.205</td>
</tr>
<tr>
<td>Max improvement</td>
<td>7.182</td>
</tr>
</tbody>
</table>

- Results of encoding public available VQEG YUV sequences

Encoder bandwidth requirement 148MB/sec
## Diamond 388VDO Performance

<table>
<thead>
<tr>
<th>Standard</th>
<th>Resolution</th>
<th>Frames per sec</th>
<th>Bit Rate</th>
<th>DDR Memory Bandwidth</th>
<th>Required clock rate</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Decode</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>H.264 Main Profile Decode</td>
<td>D1</td>
<td>30</td>
<td>5 Mbps</td>
<td>86.3 MB/s</td>
<td>162 MHz</td>
</tr>
<tr>
<td>VC-1/WMV9 Main Profile Decode</td>
<td>D1</td>
<td>30</td>
<td>6 Mbps</td>
<td>88.9 MB/s</td>
<td>172 MHz</td>
</tr>
<tr>
<td>MPEG-4 Advanced Simple Profile Decode</td>
<td>D1</td>
<td>30</td>
<td>6 Mbps</td>
<td>59.8 MB/s</td>
<td>167 MHz</td>
</tr>
<tr>
<td>MPEG-2 Main Profile Decode</td>
<td>D1</td>
<td>30</td>
<td>8 Mbps</td>
<td>46.1 MB/s</td>
<td>151 Mhz</td>
</tr>
<tr>
<td><strong>Encode</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>MPEG-4 Advanced Simple Profile Encode</td>
<td>D1</td>
<td>30</td>
<td>4 Mbps</td>
<td>148 MB/s</td>
<td>188 Mhz</td>
</tr>
</tbody>
</table>

- Bit Stream: Mobile Calendar
- Memory Latency = 32
Summary of Diamond 388VDO

- **Flexibility**
  - Full software programmability allows easy adaptation to rapidly evolving video standards and solutions

- **Low cost**
  - Hits performance goals in mature, low-cost 130nm G process
  - Small footprint (size < 11mm² in 130nm G)

- **Low clock rate** (< 200MHz)

- **Low external H.264 decoder memory bandwidth requirement** (< 90MB/s)

- **Available: NOW**