FEATURES:

- Smallest, lowest-power Linux-ready CPU in its class
- Linux-compatible Memory Management Unit
- 5-stage pipeline
- Dhrystone 2.1: 1.38 DMIPS/MHz
- 32x32 multiplier and 32-bit integer divider
- Single cycle 16x16-bit MAC
- 16-bit DSP instructions
- 16Kbyte, 4-way set associative instruction and data caches
- 32-bit input/output GPIO pins for direct communication
- Integrated interrupt controller with 22 interrupts at 6 priority levels
- Three integrated timers
- On-chip debugging hardware
- Embedded trace support
- Comprehensive software design environment
- AHB-lite and AXI bridges

The Diamond Standard 232L is a high-performance, versatile fully synthesizable 32-bit RISC CPU controller core. It is area and power efficient with a local memory architecture that provides outstanding flexibility and performance, with a full-featured Memory Management Unit (MMU) for application processing using operating systems such as Linux. The caches are 16Kbyte instruction and data, 4-way set associative.

The MMU provides instruction and data Translation Lookaside Buffers (TLBs), which manage virtual-to-physical address mapping. In addition to address translation, the MMU provides four different privilege levels (for memory protection), variable page sizes, and multiple access modes. Combining the MMU with a flexible interrupt architecture and high performance, the Diamond 232L can easily meet the needs of a complex system running numerous operations.

Arithmetic and DSP hardware support in the processor reduces the need to include a separate DSP in the system design. Arithmetic support is provided by a built-in 32x32 multiplier and 32-bit integer divider. DSP support in the Diamond 232L consists of a single-cycle 16x16-bit MAC unit adding four dedicated 32-bit registers and a 40-bit accumulator. Additionally, there is support for zero overhead looping, clamps (saturating arithmetic), max/min value, normalize, and sign extend.

BENEFITS:

- Flexible memory architecture adaptable to an extremely wide range of applications
- On-chip debug decreases time to market
- High arithmetic and DSP performance, eliminating need for separate DSP
- Fast and flexible interrupt handling
- High performance on general-purpose code
- No memory contention between instructions and data
- Ready for Linux operating system support
- Drop into existing AMBA™ systems

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Dhrystone: 1.38 DMIPS/MHz

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<thead>
<tr>
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<th>130G</th>
<th>90G</th>
<th>65GP</th>
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<tbody>
<tr>
<td>Representative Performance/Area/Power</td>
<td>Speed Optimized</td>
<td>Area Optimized</td>
<td>Speed Optimized</td>
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<tr>
<td>Area (mm²) post-synthesis</td>
<td>0.92</td>
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<tr>
<td>Cell area (mm²) post-layout</td>
<td>1.16</td>
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<tr>
<td>Frequency (MHz) post-layout</td>
<td>215</td>
<td>125</td>
<td>350</td>
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<tr>
<td>Power (mW/MHz) post-layout</td>
<td>0.274</td>
<td>0.21</td>
<td>0.12</td>
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</tbody>
</table>

130G and 90G are with TSMC Sage-X libraries.
65GP is with TSMC Advantage library, Regular Vt.
Area and frequency at worst operating condition (0.9 * Vdd, 132 C)
Power at typical operating condition (1.0 * Vdd, 25 C)
Instruction Set Architecture

The Diamond Standard Series implements the Xtensa® Instruction Set Architecture (ISA) a 32-bit RISC architecture featuring a compact instruction set optimized for embedded designs. The architecture has: a 32-bit ALU; 16, 32, or 64 general-purpose physical registers; six special purpose registers; and 80 base instructions. The Xtensa ISA employs 24-bit instructions with 16-bit narrow encodings for the most common instructions. These 16-and 24-bit instruction words are freely intermixed to achieve higher code density without compromising application performance. The Xtensa ISA thus optimizes the size of the program instructions by minimizing both the static number of instructions (the instructions that constitute the application program) and the average number of bits per instruction.

The use of 24- and 16-bit instruction words, the use of compound instructions, the richness of the comparison and bit-testing instructions, zero-overhead-loop instructions, register windowing, and the use of encoded immediate values all contribute to the Diamond processors’ small code size. Thus, the 24-/16-bit Diamond processor ISA enables designers to achieve 25% to 50% lower code size compared to conventional 32-/16-bit ISA-based RISC cores. Reducing code size results in smaller memory sizes and lower power dissipation – key parameters in cost-sensitive, highly integrated SOC designs.

The Xtensa ISA also provides powerful compare-and-branch instructions, zero-overhead loops, and bit manipulations including funnel shifts and field-extract operations.

Comprehensive Software Tool Support

A full-featured development environment – the Xtensa Xplorer™, Diamond Edition – provides a graphical user interface (GUI) to all code development tools. The compiler toolchain and instruction set simulator (ISS) are available through the GUI in addition to performance modeling tools. Based on the Eclipse framework, Xtensa Xplorer allows developers to quickly evaluate code on the pipeline-accurate ISS and interface to emulation and hardware development boards. Xtensa Xplorer serves as the cockpit for the entire development experience and integrates the compiler toolchain as well as the ISS and interfaces to hardware emulation/development boards.

Tensilica’s XCC C/C++ compiler is an optimizing compiler that employs sophisticated multi-level optimizations to increase code execution performance and reduce code size.

Also included in the Xtensa Xplorer environment are a software project manager, code profiling tools, a source code editor, a debugger, a performance-modeling tool, the Xenergy energy estimation tool, a cache performance explorer, and graphical visualization tools. Tensilica also provides both a C-based modeling environment called XTMP and SystemC models of the Diamond processors. For fast-functional simulation, Tensilica offers TurboXim, which offers 40-80x faster simulation than the ISS. See Tensilica’s Software Developer’s Toolkit product brief for more information.